1. Introduction

In order to guarantee the high standards of reliability and quality in ICs supplied by Winbond, we have established an on-going re-liability and quality monitoring program. Monitor testing is performed across all product lines in a regular basis. Test results are subsequently made available in a quarterly report. This re-port details all the test results performed in the previous one quarter, outlining the reliability data associated with all process/package family types.

Since it was founded in September 1987, Win-bond has stressed product research and develop-ment (R&D), investing an average of 10% of an-nual revenues in R&D. The R&D staff includes individuals with expertise in the design of memory ICs, microcomputer and peripherals ICs, communications ICs, and many other product ar-eas. This wide range of expertise enables Win-bond's R&D team to develop more than twenty new products each year.

Winbond strives to continuously improve the quality and reliability of its products by conduct-ing failure analysis on failed parts identified in reliability tests and by customers to discover fail-ure modes and propose corrective action. To this end, a sophisticated failure analysis laboratory has been set up at Winbond headquarters. Detailed information on failure analysis procedures will be presented in this report.

2. Quality and Reliability Organization

The Quality and Reliability Assurance Division at Winbond reports directly to the President's Office. One of the division's main responsibilities is to determine quality policies and programs at the corporate level and then apply them to worldwide operations. In cooperation with other departments, the Quality and Reliability Assurance Division is also responsible for product quality and reliability monitoring and improvement programs, which ensure that products shipped out are of high quality and satisfy customers' needs. The organization of the Quality and Reliability Assurance Division is depicted in the chart in Figure 2.1, which also lists the major responsibilities of each department within the division.

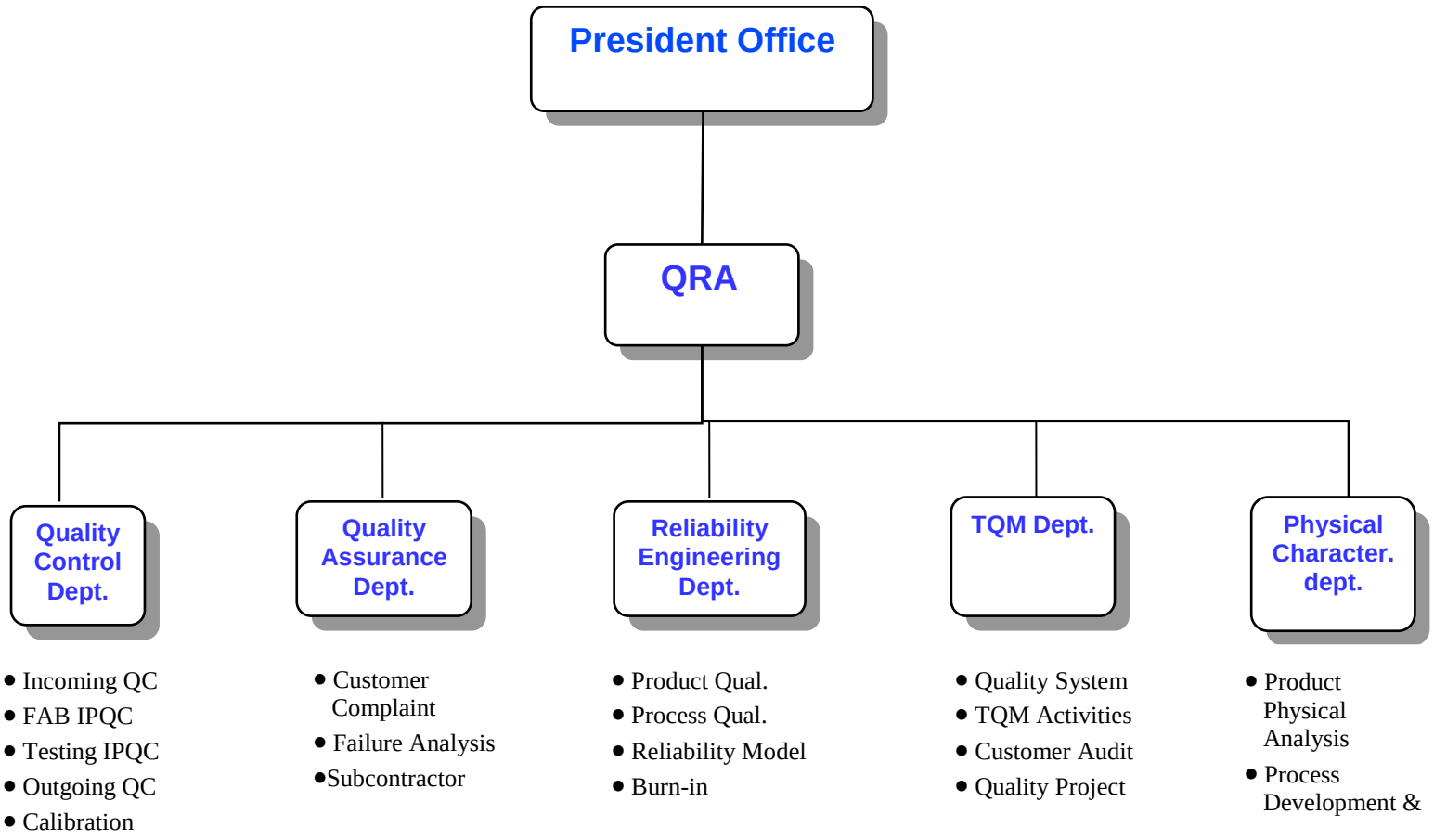

Figure 2.1 Organization Chart and Job Coverage of Quality and Reliability Assurance Division

3. Quality Management

Quality Policy

To become a world class company offering products/services that best satisfy our customers, by establishing Total Quality Management and Quality Comes First corporate culture through the process of continuous improvement.

Built-in Quality

At Winbond, we recognize that every phase of the development and manufacturing process inevitably affects the quality and reliability of the final products, so we concentrate on building quality and reliability into our products from the start. Our commitment to quality is fundamental to our long-term success, so all employees at Winbond participate in quality and reliability assurance activities as part of their basic job responsibilities. Every function and every individual is accountable for a defect-free operation.

Our Commitment to Quality and Reliability

Winbond is committed to manufacturing VLSIs with superior quality and reliability. We maintain high standards and rigid specification control throughout all the steps in the manufactur-ing process.Through continuous research and development activities and process improvement, we strive to establish and maintain increasingly higher standards of quality and reliability.

Quality Certificate

To verify that its committed to maintain world-class quality standards is realized in practice, Winbond has obtained certification from the world's leading quality control promotion organizations. In 1993, we were proud to be certified as an approved manufacturer under both the IECQ and ISO 9002 systems, and in 1994 we were certified under the ISO 9001 system.

Quality Management Program

The purpose of Quality Management Program at Winbond is to establish the controls needed to assure that the quality and reliability of our VLSI products fully satisfy our customers. We strive to deliver competitive products free from defects and to provide our customers with prompt, professional service. Our Quality Management

Program focuses on three major areas: quality control, reliability assurance, and failure analysis. Figure 3.1 shows the Winbond quality assurance system flow chart.

Quality Control

Winbond has implemented a series of quality control functions that cover all the steps in manufacturing process. The main steps in this quality control procedure are:

- Incoming materials inspection
- Wafer processing
- Electrical characteristics testing
- Chip assembly

Constant monitoring on all steps in the manufacturing process and information feedback at all levels allow fast and efficient detection of problems, evaluation and analysis, and corrective measures. We emphasize that each step in the manufacturing process should be undertaken with a "Do it right at the first time" attitude and must produce a defect-free output. The over-all result is a line of high-quality, reliable products.

Reliability Assurance

At Winbond, the aim of reliability assurance testing is to assure high-level product performance throughout the intended life of the products. Each manufacturing phase is subject to continuous review, analysis, and evaluation, with modifications introduced to further improve quality and reliability. Our reliability system is based on three important sources of reliability data:

- Release qualification tests
- Real time monitor and conformity tests
- Field failure information

Failure Analysis

Failure analysis, which determines the cause of product failures and proposes corrective action, is an important part of reliability assurance. At Winbond, scanning electron microscopes, diagnostic probe stations, optical microscopes, and many other precision instruments are used to perform failure analysis on devices submitted from various sources. Defective ICs are logged into the laboratory for inspection and for preparation of corrective action reports.

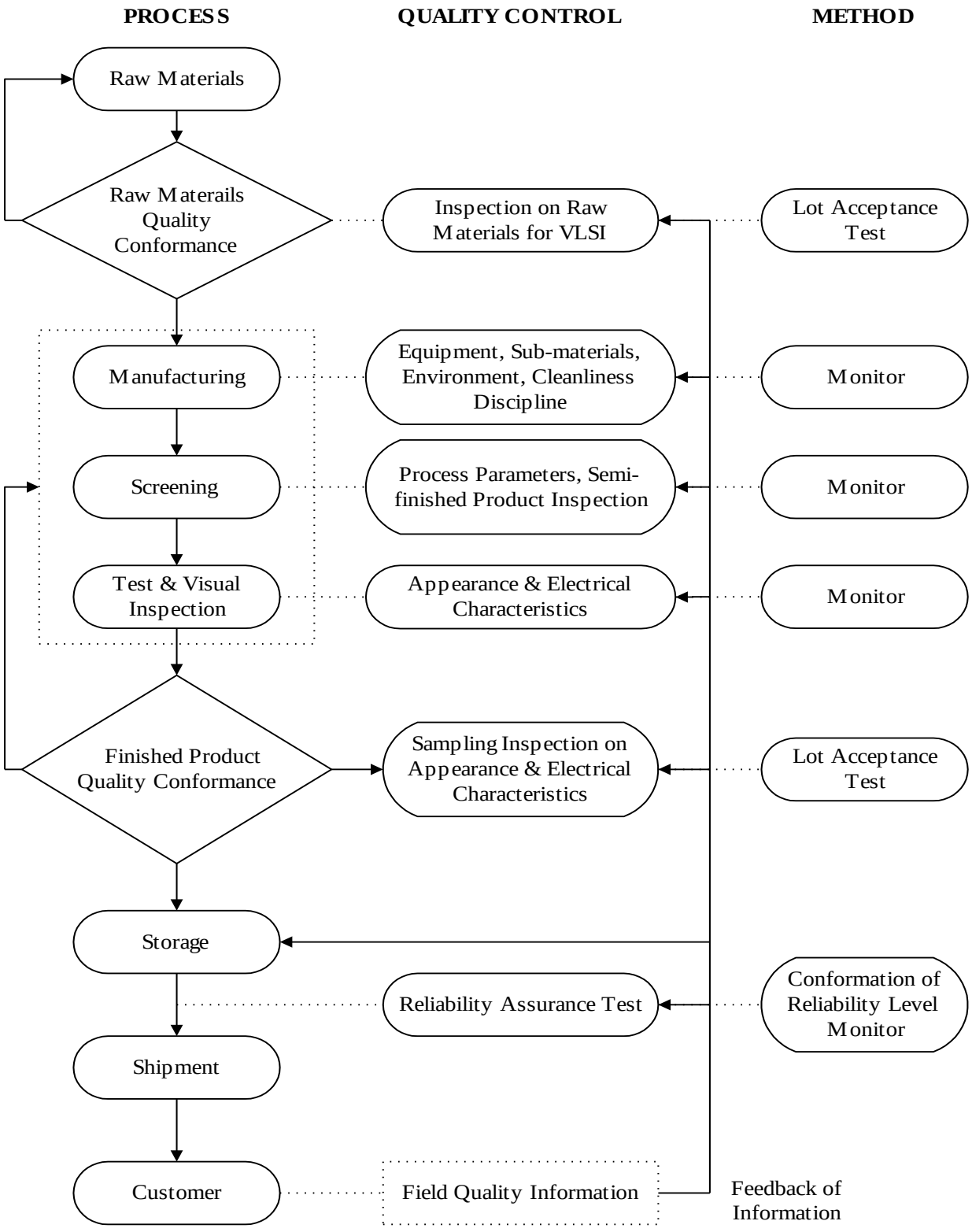

Figure 3.1 Winbond Quality Assurance System Flow Chart

4. Customer Return Handling Flow and Failure Analysis Procedures

Customer Return Handling Flow

To ensure that customers receive prompt and efficient service, Winbond has developed a detailed procedure for handling products returned by customers (see Figure 4.1). Field quality information is an essential factor in improving product quality. Field failures are subjected to detailed failure analysis, the results of which are used to propose corrective action for implementation in design, production, or testing.

Failure Analysis Procedures

A successful failure analysis should indicate the root cause of failure and suggest appropriate corrective measures. Since ICs are subject to a wide range of failure modes, which may be caused by a variety of factors, Winbond has established a comprehensive failure analysis procedure to guide the analysis and evaluation of all rejected products. Failure analysis is generally conducted in Winbond's sophisticated in-house failure analysis laboratory; in special cases, failure analysis work may also be subcontracted to outside labs. Figure 4.2 depicts the general failure analysis procedure.

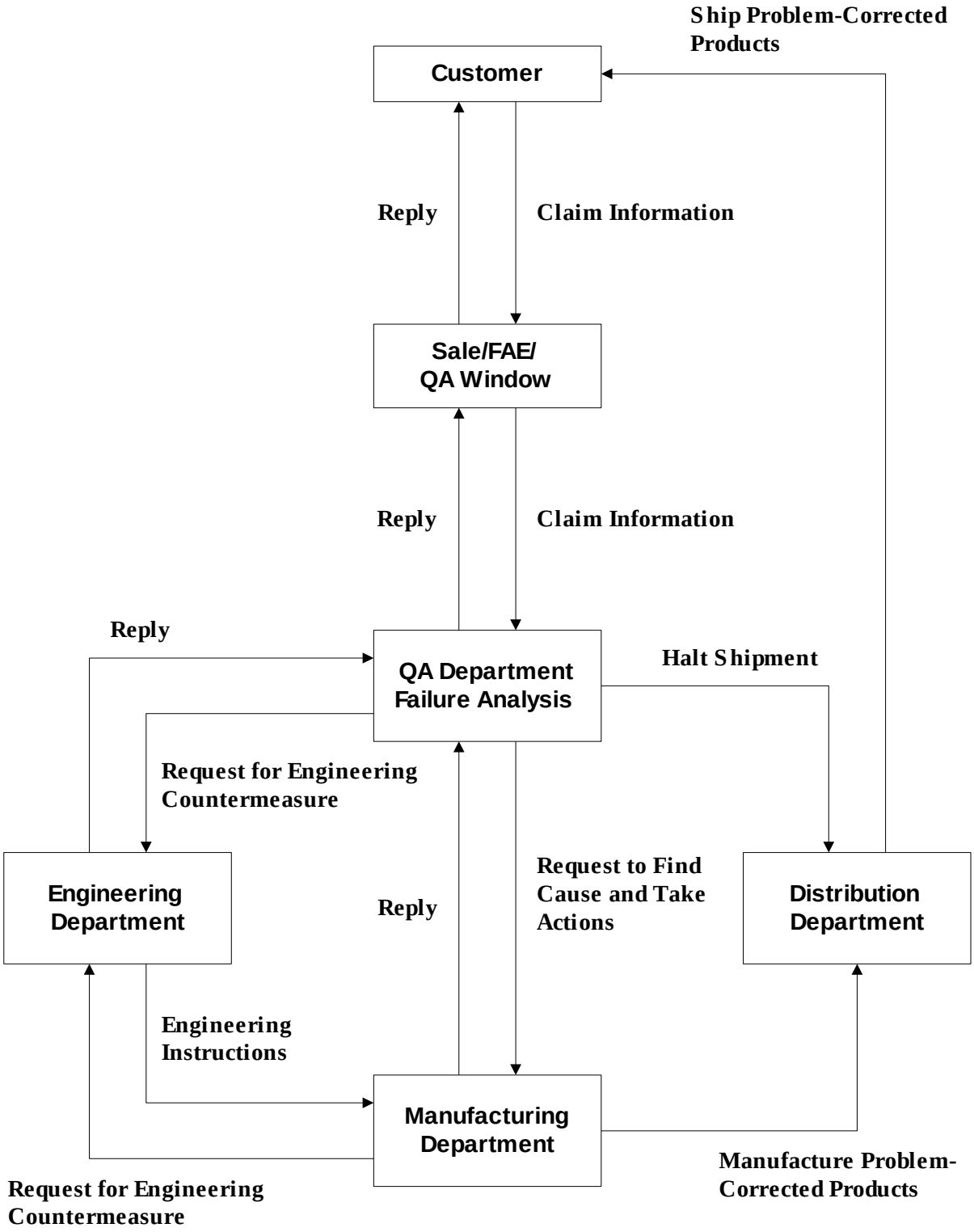

Figure 4.1 Customer Claim Processing Flow

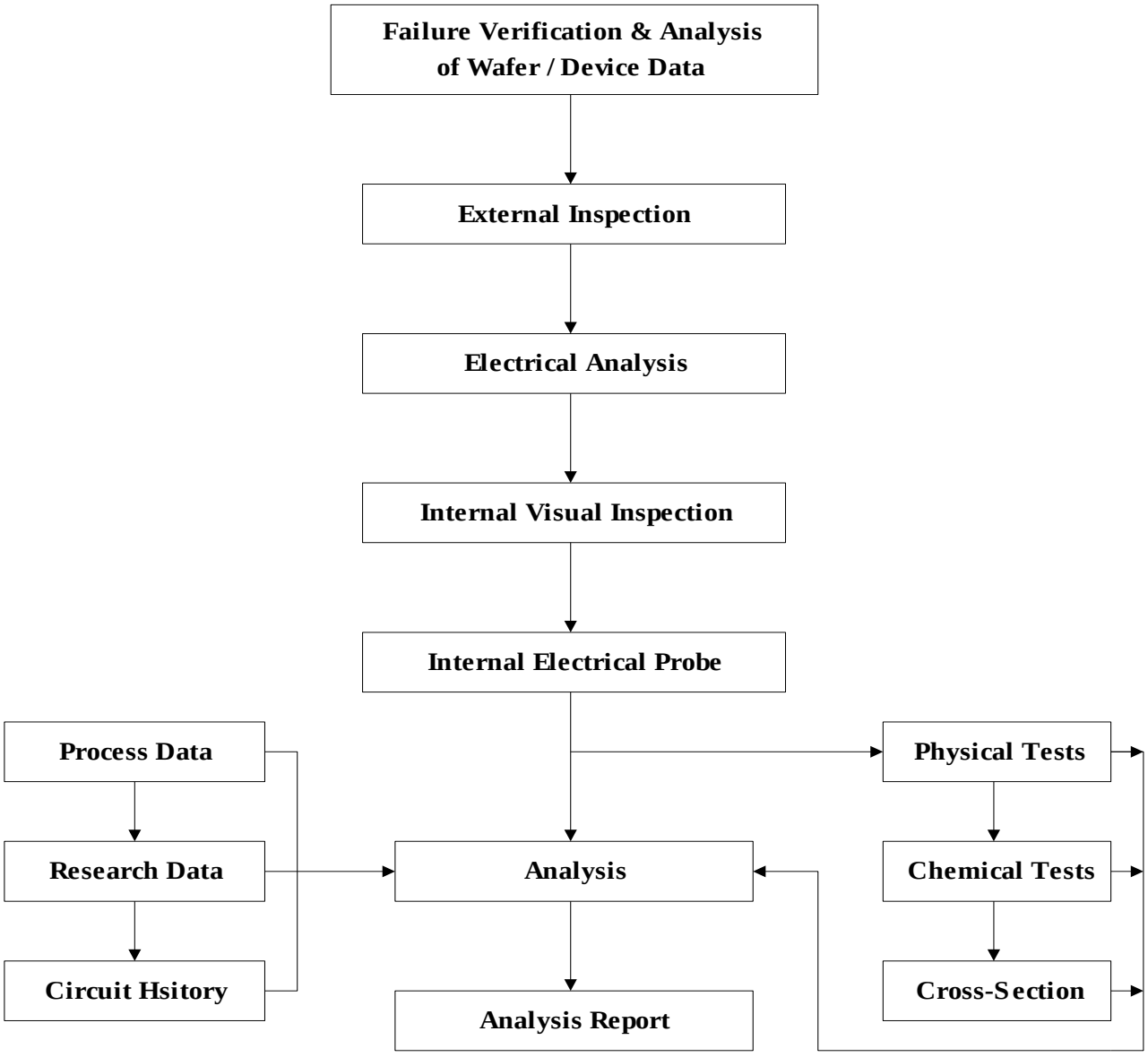

Figure 4.2 Failure Analysis Procedure

5. Reliability Testing

The purpose of reliability testing is to ensure that products are properly designed and assembled by subjecting them to stress conditions that accelerate potential failure mechanisms. Reliability test methods are defined in many industrial standards, such as MIL-STD-883, the main source of the methods applied in reliability testing at Winbond. In this report, reliability tests have been divided into three categories: process-related reliability tests, package-related reliability tests, and device reliability tests.

Process-Related Reliability Tests

Dynamic Early Fail Study (EFR)

The purpose of the dynamic early fail study (EFR) is to estimate the infant mortality failure rate that occurs within the first year of normal device operation by accelerating infant mortality failure mechanisms. Typical stress temperature is set to 125 °C at nominal voltage (3.6 V for 3.3V FLASH; 4.6V/3.8V/1.95V for 3.3V/3.3V/1.8V DRAM). The duration is 96/72/16/5 hours.

High-Temperature Operating Life Test (HTOL) (JESD22-A108)

The purpose of the high-temperature operating life (HTOL) test is to determine the reliability of Products by accelerating thermally activated failure mechanisms by subjecting samples to extreme temperatures under biased operating conditions. The test is used to predict long-term failure rates in terms of FITs (failures in time), with one FIT representing one failure in 10^9 device hours. All test samples are screened directly after final electrical testing. The oven temperature for the HTOL test is 125 °C. Testing is performed with dynamic signals applied to the device, and the typical Vcc is the maximum operating voltage.

Non-Volatile Memory Cycling Endurance (NVCE) (JESD47F and JESD22-A117A)

The non-volatile memory cycling endurance test is to measure the endurance of the device in program and erase cycles. Half of the devices are cycled at room temperature (25℃), and half at high temperature (85℃). The numbers of blocks (sectors) cycled to 1k, 10k, and 100k are generally in the ratio of 100:10:1. Total cycling time is 500 hours and one-third of the cycling time is devoted to 1k, 10k, and 100k cycles count individually. For all possible failure mechanisms, such like program disturbs, gate disturbs, and program / erase ability are tested and checked on each cycle area.

Low Temperature Retention and Read Disturb (LTDR) (JESD47F and JESD22-A117A)

The NVCE devices cycled at room temperature are placed into room temperature operating life stress that sequentially performs dynamic read access on all memory address. 25℃stress temperature is used to determine sensitivity to non-temperature accelerated retention failure mechanisms, or to mechanisms that can entirely recover at high temperature, such as the SILC mechanism. Biased life stress is performed to detect voltage-induced disturbs due to random bit accesses, in addition to unbiased data retention mechanisms which occur when a bit is not being accessed.

High Temperature Data Retention (HTDR) (JESD47F and JESD22-A117A)

The NVCE devices cycled at high temperature are placed in high-temperature retention bake with no electrical bias. Blocks or sectors cycled to 1k and 10k cycles are required to retain data for 100 hours of 125℃ bake, and blocks or sectors cycled to 100k cycles must retain data for 10 hours of 125℃ bake.

Electrostatic Discharge (ESD) Test

The electrostatic discharge test measures the sensitivity of each device pin to electrostatic discharges that might occur during handling. At Winbond, ESD is evaluated by using the human body model (JESD22-A114) with C = 100 pF and R = 1.5 K to simulate discharge through human contact.

Latch-Up Test

The latch-up test is a special test used with CMOS processes to detect parasitic bipolar circuits that can short the power and ground nodes when they are activated. Winbond adopts JEDEC -78 standards: The current is applied to each I/O pin in steps while the power supply current is monitored. The current into the test pin must rise to a minimum of 100 mA without latch-up occurring.

Package-Related Reliability Tests

Preconditioning

The purpose of preconditioning is to measure the resistance of surface mount devices to the storage environment at the customer site and to thermal stress created by IR reflow or vapor phase reflow. Before they undergo the temperature-humidity-bias test, the temperature cycle test, the thermal shock test, the pressure cooker test or the highly-accelerated temperature and humidity stress test, surface mount devices are subjected to preconditioning and must then pass a final electrical test. The steps of precondition for DRAM, non-volatile and logic:

Step1: Temperature Cycle Test (-65 °C /150 °C), 5 cycles.

Step 2: Bake for 24 hours at 125 °C.

Step 3: Soak for 192 hours at 30 °C/RH60%. (for 52 hours at 60 °C/RH60%).

(JEDEC LEVEL III)

Step 4: IR Reflow, 3 passes.

High-Temperature Storage Life Test (HTSL)
(JESD22-A103)

The high-temperature storage life test measures device resistance to a high temperature environment that simulates a storage environment. The stress temperature is set to 150°C to accelerate the effect of temperature on the test samples. In the test, no voltage bias is applied to the devices.

Temperature Cycle Test (TCT)
(JESD22-A104)

The purpose of temperature cycle testing is to study the effect of thermal expansion mismatch among the different components within a specific die and packaging system. The cycling test system has a cold dwell at – 65°C and a hot dwell at 150 °C, and it employs a circulating air environment to ensure rapid stabilization at a specified temperature. During temperature cycle testing, devices are inserted into the cycling test system and held at cold dwell for 15 minutes, and then the devices are heated to hot dwell for 15 minutes. One cycle includes the duration at both extreme temperatures and the two transition times. The transition period is less than one minute at 25 °C. The test duration is 200 cycles for non-volatile and logic, 500 cycles for DRAM. Samples of surface mount devices must first undergo preconditioning and pass a final electrical test prior to the temperature cycle test.

Pressure Cooker Test (PCT)
(JESD22-A102)

The pressure cooker test is an environmental test that measures device resistance to moisture penetration and the effect of galvanic corrosion. The stress conditions for the pressure cooker test employed at Winbond are 121 °C (for non-volatile, logic and for DRAM) and 100% relative humidity. The duration of the test is 168/300 hours. Samples of surface mount devices are subjected to preconditioning and a final electrical test prior to the pressure cooker test. After the pressure cooker test, the leads of the test samples are cleaned and then baked at 150 °C for 1 hour before the final electrical test.

Highly-Accelerated Temperature and Humidity Stress Test (HAST) (JESD22-A110)

The highly accelerated temperature and humidity stress test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state device in an environment with high humidity. It employs severe condition of temperature, humidity, and bias, which accelerate the penetration of moisture through the external protective material (encapsulated or seal) or along the interface between the external protective material and the metallic conductor, which pass through it. Samples of surface mount devices are subjected to preconditioning and a final electrical test prior to the highly-accelerated temperature and humidity stress test. The stress conditions of the HAST test employed at Winbond are 130 °C, 85% RH, 2 atm and Vdd = maximum operating voltage and pin combination bias. The duration of the test is 168 hours for nov-volatile, and logic and 300 hours for DRAM.

Device Reliability Tests

Electromigration (EM) Test

Electromigration is the motion of interconnect metallization due to momentum exchange from the electron current. A convergence of metallic ion flux can lead to hillock formation, which may result in short circuits to adjacent or overlaying conductors. A divergence of the metallic ion flux can lead to void formation, which may result in open circuit failure. In the electromigration test, specially designed test structures are stressed by high-current densities and high temperature to accelerate the electro-migration process. The stress temperature is 235 °C for DRAM and FLASH process. The stress current density is about 10^6 Amp/cm^2. A test sample is defined as a failure if its resistance variation is more than 10% of its initial resistance. Regression analysis is used to find the best fit of lognormal distribution data so as to calculate the median time-to-failure(MTF) under the stress conditions. Then, by multiplying the temperature and current acceleration factors, we can find the MTF due to electro-migration under use condition. Lifetime(τ) is specified as $\tau_{0.1\%} \geq$ 10 years @130°C for the DRAM and FLASH process.

Stress Migration(SM) Test

The purpose of the test is to see if the stress cause inadmissible resistance variation. The stress temperature is 250°C and the criterion is specified as ΔR <10% after 1000Hrs stress.

Bias Temperature (BT) Test

The purpose of the test is to investigate the degradation during the bias temperature stress due to ionic contamination or increased positive charge. The stress condition for the test is stressed by 1.5~2V_{DD} @ 85~150°C and the sample failure definition is >10% Ids. And criterion is AC lifetime should be larger than 10years @Vd=1.1V_{DD}.

Hot Carrier Effect (HCE) Test

Hot carrier effects occur in most transistors when the lateral electric field in the drain depletion region or in the channel becomes so large that the major carriers in the channel gain energy from the electric field faster. These carriers may gain enough energy (1.5 eV) to impact-ionize and create hole-electron pairs, which results in a measurable substrate current consisting of carriers with opposite charge to the major carriers in the channel. If the hot carriers further gain enough energy (3-4 eV), they can overcome the $Si\text{-}SiO_2$ barrier and be injected into the oxide layer. In the HCE test, the test MOS transistors are divided into three groups, which are DC-stressed under three different values of Vd higher than the maximum operating voltage. Three different values of Vd before Id becomes infinity as Vd increases are chosen as the three stress voltages. The gates of the test transistors are biased at the value such that Isub is the maximum value in Isub vs. Vg for NFET and the maximum value in Ig vs. Vg for PFET, repectively. The stress temperature is room temperature. A test sample is defined as a failure if the variation in I_{dsat} is more than 10% of its initial value for NFET, or the variation in Vth is more than 100mV for PFET. The lifetime τ is specified as $\tau_{AC} \geq 10$ years.

Charge to Breakdown (QBD) Test

The purpose of the QBD test is to measure the breakdown charge density of the gate oxide. In the test, a constant current density is applied to a test sample until it breaks down. The stress current density is 0.1 Amp/cm^2. To pass the test, the breakdown charge density of a test sample must be larger than 1 Coul/cm^2 at weibull 63%.

TDDB Test

The oxide will only allow a finite amount of charge to pass it before it breakdown. The purpose of TDDB testing is to characterize when this breakdown occurs and to evaluate oxide lifetime. Regression analysis is used to find the best fit of Weibull distribution data so as to calculate the median time-to-failure(MTF) under the stress conditions(here is Vuse@85C/125C and normal operation conditions. The lifetime criterion is specified as $\tau \geq 10$ year @85°C under normal operation voltage.