Application Note-02

PROGRAMMING W29C/W29EE FLASH FAMILY

GENERAL DESCRIPTION

As the industry recognizes the benefits of field reprogrammablity for system, the need for a cost effective, easy to update non-volatile memory rises. The Flash memory has shown great promise to become the memory of choice. Winbond offers to our customers with W29C/W29EE Flash memory family.

One concern of system designers when using nonvolatile programmable memories is the possibility of inadvertent write operation that can be caused by noise or by power-up and power-down sequences. Winbond's Flash memories provide a feature called SDP-Write (Software Data Protection Write) that addresses this issue. Once SDP has been enabled, the device requires all subsequent write operations to perform a series of commands before loading the chosen page with data. The command consists of loading three pre-defined data values into three predefined addresses. This 3-byte loading sequence proceeding a write operation virtually eliminates the possibility of inadvertent write operations. The SDP-Write sequence is described below:

1. Loading Data AA (hex) into Address 5555 (hex)
2. Loading Data 55 (hex) into Address 2AAA (hex)
3. Loading Data A0 (hex) into Address 5555 (hex)
4. Loading desired page with data
5. Pause 10 mS (Twc: write cycle time)
6. Continue with next operation

Once SDP is enabled, any write operation attempt to the device without loading the proceeding 3-byte command sequence would not initiate the internal non-volatile memory programming operation, and no data will actually be written to the device; however, during this write cycle time (Twc), valid data cannot be read from the Flash. Furthermore, the Software Data Protection feature will remain enabled and the Flash device is under write protection unless the 6-byte disable command was issued. For your reliable applications, Winbond recommends that SDP-Writes are used for all Flash write operations.

In order to maximize the reliability of the applications, special precautions must be applied at the system level during power-up period. It is necessary that the Chip-Enable pin ($\overline{CE}$) and the Write-Enable ($\overline{WE}$) pin are kept at high level (or follow Vdd supply voltage level) during power supply (V_{DD}) ramp-up period to avoid inadvertent write operations since the internal write protection status could temporarily be destroyed during this period. It is also highly recommended that external pull-up resistor(s) is/are connected to the Chip-Enable and/or Write-Enable pin(s) to further minimize the possibility of inadvertent writes when these control pins are not very well controlled (or floating) during this system power ramp up period.

Due to the self-timed characteristics of the Flash device, it is required that certain time period must be elapsed before any specific operation can be performed to the Flash after power-up. Hence, the Power-up to Read (Tpu.read = 100 μS) and the Power-up to Write (Tpu.write = 5mS) must not be violated.

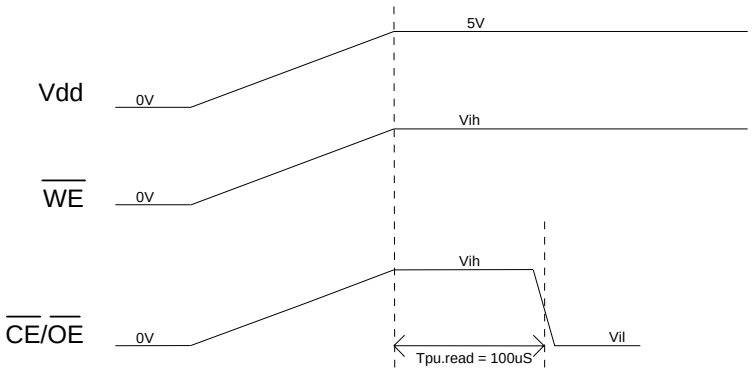

Fig.1: Power-Up to Read Operation Waveform

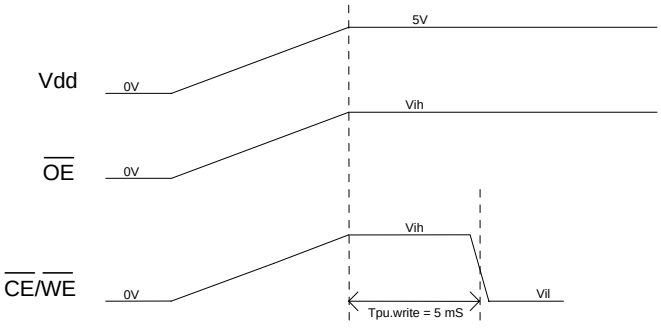

Fig.2: Power-Up to Write Operation Waveform

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Apr. 1998		Initial Issued
A2	Nov. 1998	1, 2	Adding power-up precautions & waveforms