

W25Q12PW-DTR



***spi*flash[®]**

**1.8V 128M-BIT
SERIAL NOR FLASH MEMORY WITH
DUAL/QUAD SPI & QPI & DTR**



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1. GENERAL DESCRIPTIONS

The W25Q12PW (128M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers on-chip ECC to improve memory data integrity and overall system reliability. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 1.65V to 1.95V power supply with current consumption as low as 1 μ A for power-down. All devices are offered in space-saving packages.

The W25Q12PW array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q12PW has 4,096 erasable sectors and 256 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 2.)

The W25Q12PW supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2, and I/O3. SPI clock frequencies of up to 166MHz are supported allowing equivalent clock rates of 664MHz (166MHz x 4) for Quad I/O when using the SPI Fast Read Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

The ECC enabled W25Q12PW device has additional features related to ECC and Reset functionality. These features are supplemented to support and enhance device performance in highly intensive industrial environment. With ECC enabled feature, the device supports 1 bit ECC every 16-byte alignment. The device offers internal ECC Status to monitor the ECC error.



2. FEATURES

- **New Family of SpiFlash Memories**
 - W25Q12PW: 128M-bit / 16M-byte
 - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
 - Dual SPI: CLK, /CS, IO₀, IO₁, /WP, /Hold
 - Quad SPI: CLK, /CS, IO₀, IO₁, IO₂, IO₃
 - QPI: CLK, /CS, IO₀, IO₁, IO₂, IO₃
 - SPI/QPI DTR(Double Transfer Rate) Read
- On-chip ECC(1-Bit correction every 16-Byte)^{(1) (3)}
- Buffer Mode
- **Highest Performance Serial Flash**
 - 166MHz Quad I/O clocks
 - 104MB/s continuous data transfer rate
 - Min. 100K Program-Erase cycles^{(2) (3)}
 - More than 20-year data retention⁽³⁾
- **Efficient “Continuous Read” and QPI Mode**
 - Continuous Read with 8/16/32/64-Byte Wrap
 - As few as 8 clocks to address memory
 - Quad Peripheral Interface (QPI) reduces instruction overhead
 - Allows true XIP (execute in place) operation
- **Low Power, Wide Temperature Range**
 - Single 1.65 to 1.95V supply
 - <1μA Power-down (typ.)
- -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
 - Uniform Sector/Block Erase (4K/32K/64K-Byte)
 - Program 1 to 256 byte per programmable page
 - Erase/Program Suspend & Resume
- **Advanced Security Features**
 - Software and Hardware Write-Protect
 - Power Supply Lock-Down and OTP protection
 - Top/Bottom, Complement array protection
 - 64-Bit Unique ID for each device
 - Discoverable Parameters (SFDP) Register
 - 3X256-Bytes Security Registers with OTP locks
 - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
 - 8-pin SOP 208-mil/300-mil
 - 8-pad XSON 4x4-mm / USON 4x3-mm
 - 8-pad WSON 6x5-mm / 8x6-mm
 - 24-ball TFBGA 8x6-mm
 - 16-ball WLCSP
 - Contact Winbond for KGD and other options

Note:

1. To maintain the ECC operation (ECC On Status) on aligned 16-byte memories across the full memory range (on LSB address A[3:0] = 0000b to 1111b) during reads, one time programming of one byte up to 16 bytes of data per aligned 16-Byte memory is required. More than one time programming on aligned 16-byte memories will turn off ECC functionality (ECC Off status) automatically on those affected aligned 16-byte memories during reads. An Erase is required to recover back ECC operations (ECC On Status) of these affected aligned memories during reads.
2. Qualification with 16-bytes aligned programming.
3. 16-bytes aligned programming is required to guarantee the data retention and program-erase cycles.



3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1 Pin Configuration SOP 208-mil

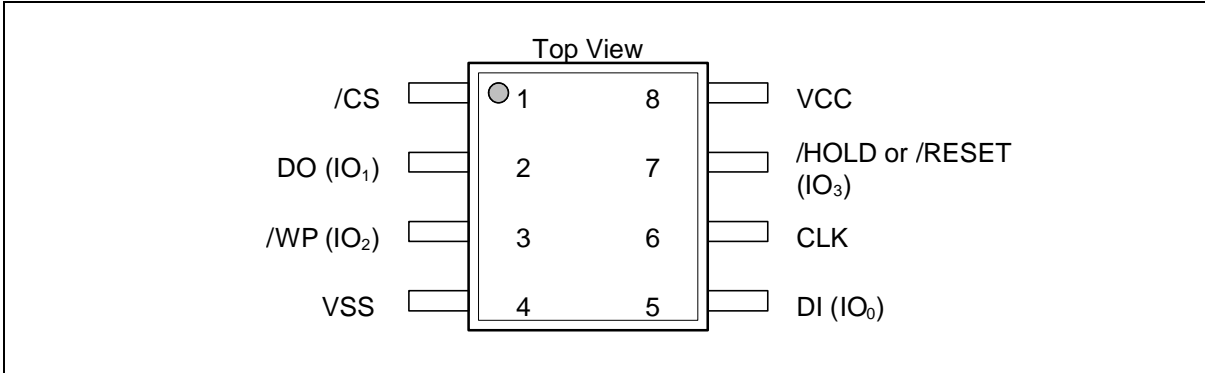


Figure 1a. Pin Assignments, 8-pin SOP 208-mil (Package Code CS/SS)

3.2 Pad Configuration USON4x3-mm, XSON4x4-mm, WSON 6x5-mm / 8x6-mm

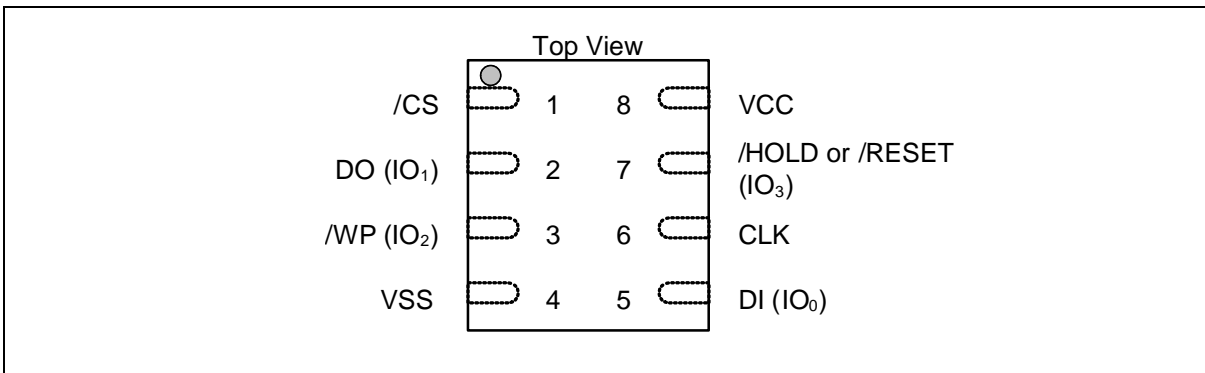


Figure 1b. Pad Assignments USON4x3-mm, XSON4x4-mm, WSON 6x5-mm / 8x6-mm (Package Code UU, XG,CP/ZP, CE/ZE)

3.3 Pin Description SOP 208-mil, USON4x3-mm, XSON4x4-mm, WSON 6x5-mm / 8x6-mm

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO ₁)	I/O	Data Output (Data Input Output 1) ⁽¹⁾
3	/WP (IO ₂)	I/O	Write Protect Input (Data Input Output 2) ⁽²⁾
4	VSS		Ground
5	DI (IO ₀)	I/O	Data Input (Data Input Output 0) ⁽¹⁾
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO ₃)	I/O	Hold or Reset Input (Data Input Output 3) ⁽²⁾
8	VCC		Power Supply

Notes: 1. IO₀ and IO₁ are used for Standard and Dual SPI instructions

2. IO₀ – IO₃ are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.



3.4 Pin Configuration SOP 300-mil

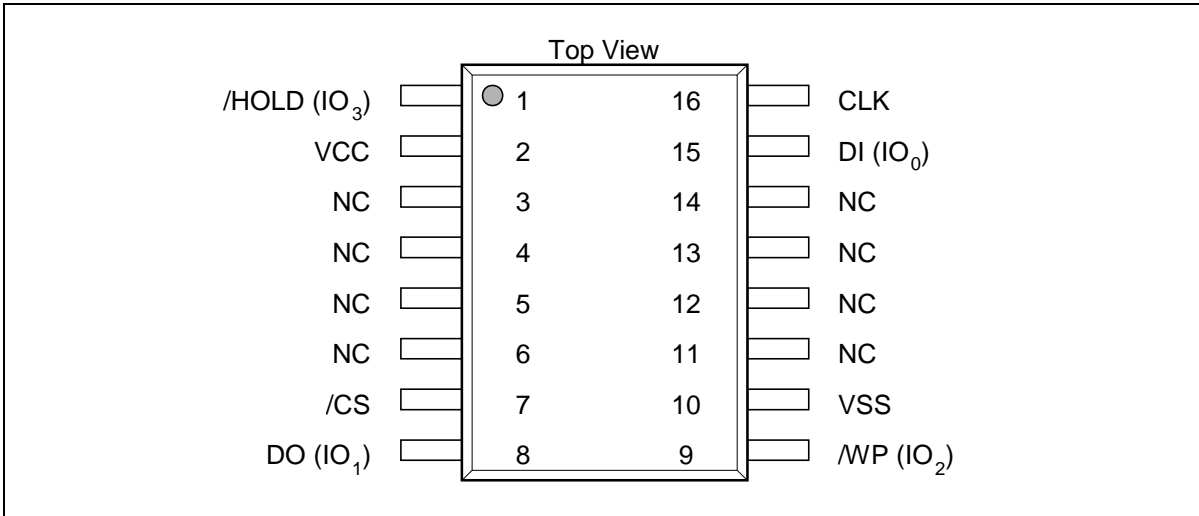


Figure 1c. Pin Assignments, 16-pin SOP 300-mil (Package Code CF/SF)

3.5 Pin Description SOP 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/HOLD (IO3)	I/O	Hold or Reset Input (Data Input Output 3) ⁽²⁾
2	VCC		Power Supply
3	N/C		No Connect
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO (IO1)	I/O	Data Output (Data Input Output 1) ⁽¹⁾
9	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2) ⁽²⁾
10	VSS		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI (IO0)	I/O	Data Input (Data Input Output 0) ⁽¹⁾
16	CLK	I	Serial Clock Input

Notes:

- IO0 and IO1 are used for Standard and Dual SPI instructions
- IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.



3.6 Ball Configuration TFBGA 8x6-mm (5x5 or 6x4 Ball Array)

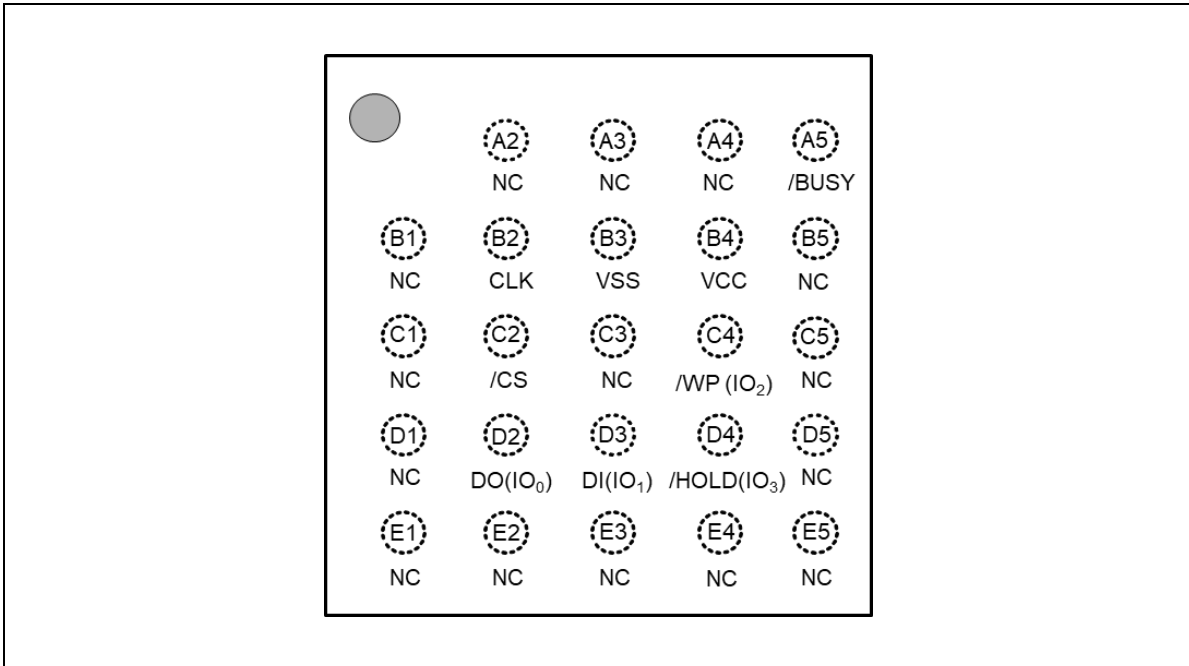


Figure 1e. W25Q12PW Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code CB)

3.7 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
A5	/BUSY	O	BUSY ⁽³⁾
B2	CLK	I	Serial Clock Input
B3	VSS		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2) ⁽²⁾
D2	DO (IO1)	I/O	Data Output (Data Input Output 1) ⁽¹⁾
D3	DI (IO0)	I/O	Data Input (Data Input Output 0) ⁽¹⁾
D4	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3) ⁽²⁾
Multiple	NC		No Connect

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO0 – IO3 are used for Quad SPI instructions

*3 The /RESISTOR pin is a dedicated hardware pin regardless of device operation states. If the hardware /BUSY function is not used, this pin can be left floating.



3.8 Ball Configuration WLCSP

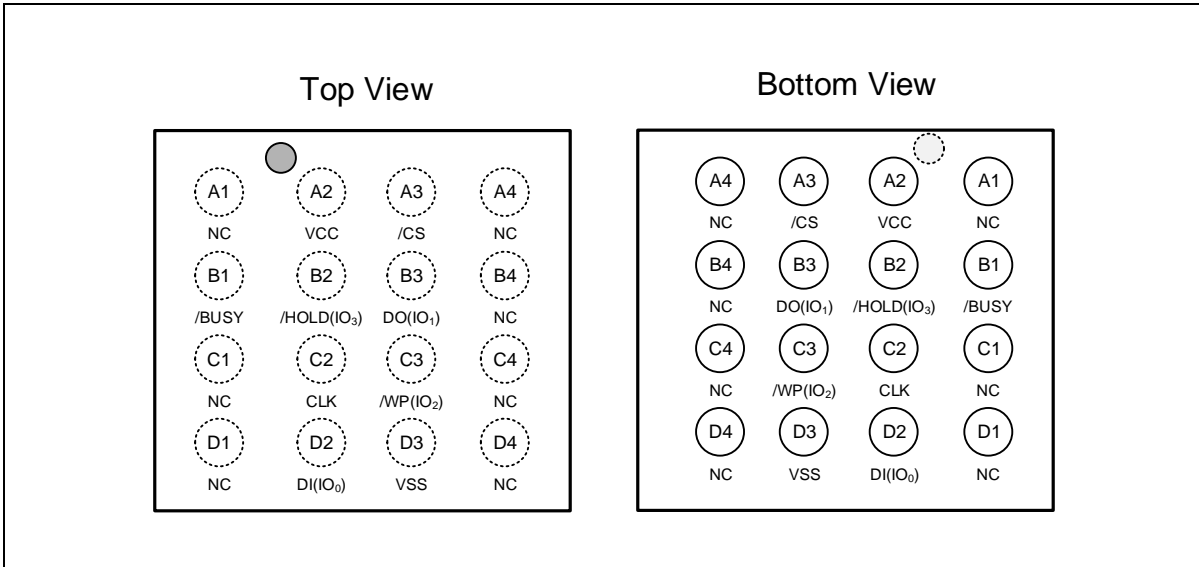


Figure 1f. W25Q12PW Ball Assignments, 16-ball WLCSP (Package Code BY)

3.9 Ball Description WLCSP

BALL NO.	PIN NAME	I/O	FUNCTION
A2	VCC		Power Supply
B2	/HOLD (IO3)	I/O	Hold or Reset Input (Data Input Output 3) ⁽²⁾
C2	CLK	I	Serial Clock Input
D2	DI (IO0)	I/O	Data Input (Data Input Output 0) ⁽¹⁾
A3	/CS	I	Chip Select Input
B3	DO (IO1)	I/O	Data Output (Data Input Output 1) ⁽¹⁾
C3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2) ⁽²⁾
D3	VSS		Ground
B1	/BUSY	O	BUSY
Multiple	NC		No Connect

Notes:

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO0 – IO3 are used for Quad SPI instructions



4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high, the device is deselected, and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the device's power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low, before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see "Write Protection" and Figure 58). If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q12PW supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and the /HOLD pin becomes IO3.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See Figure 1a-c for the pin configuration of Quad I/O operation.

4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See Figure 1a-e for the pin configuration of Quad I/O operation.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

4.6 BUSY PIN (/BUSY)

For the WLCPS/KGD package, W25Q12PW provides a dedicated /BUSY pin. The /BUSY pin is an asynchronous Ready/BUSY# signal. /BUSY pin has an open drain and an internally pulled up driver. The /CS pin does not need to be asserted (device selected) to get the Ready/Busy# status. When the /BUSY pin is low, the device is busy with an internal program, erase, or write operation. When the /BUSY pin is high, the device is not performing any internal program, erase, or write operation.



5. BLOCK DIAGRAM

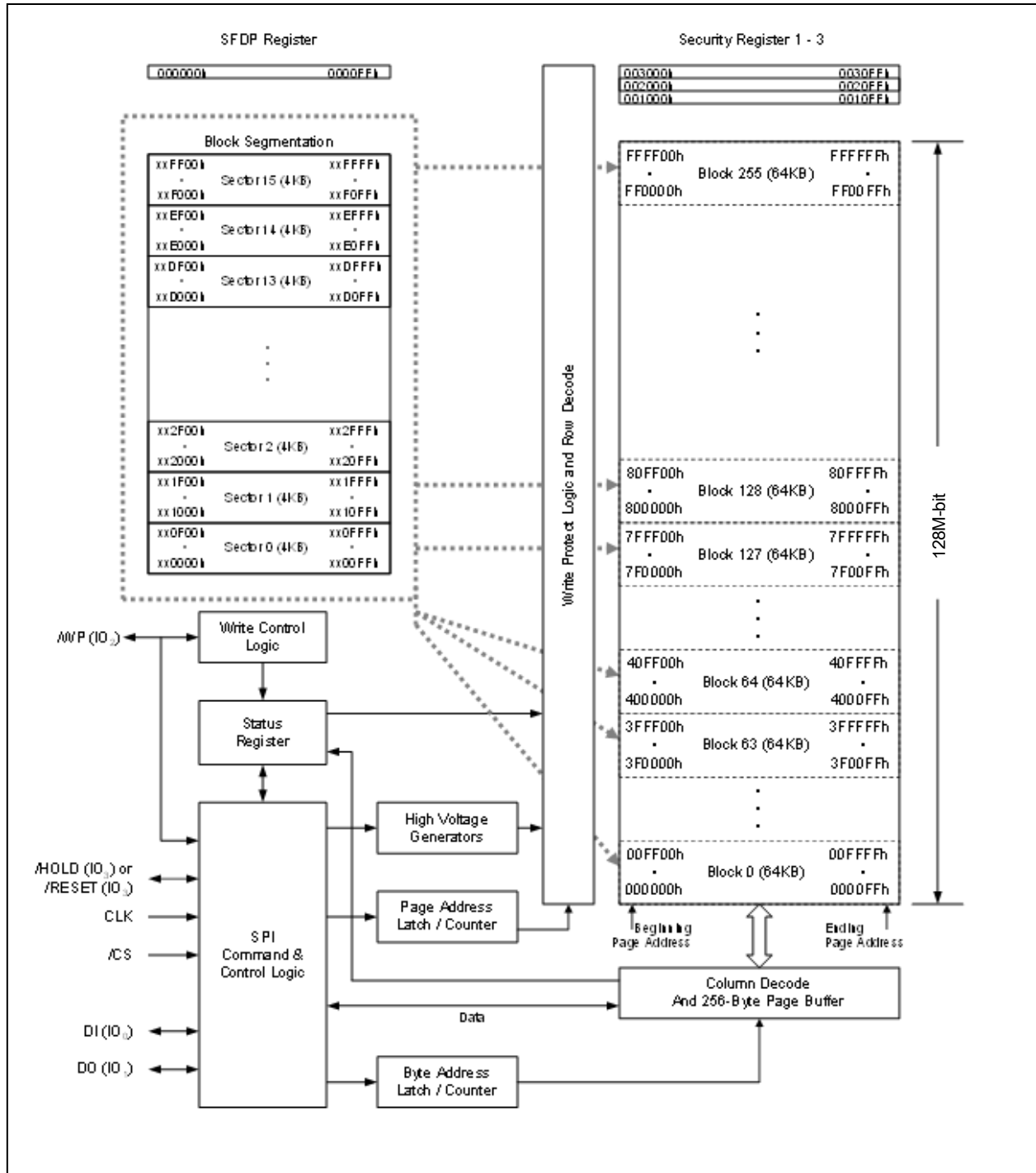


Figure 2. W25Q12PW Serial Flash Memory Block Diagram



6. FUNCTIONAL DESCRIPTIONS

6.1 SPI / QPI Operations

6.1.1 Standard SPI Instructions

The W25Q12PW is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.2 Dual SPI Instructions

The W25Q12PW supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.1.3 Quad SPI Instructions

The W25Q12PW supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions, offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.1.4 QPI Instructions

The W25Q12PW supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code is shifted into the device using only the DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus, only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” instruction, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See Figure 3 for the device operation modes.

6.1.5 SPI / QPI DTR Read Instructions

To effectively improve the read operation throughput without increasing the serial clock frequency, W25Q12PW introduces multiple DTR (Double Transfer Rate) Read instructions that support

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Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

6.1.6 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25Q12PW operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. If the page buffer was only partially written when a priority interrupt requires use of the SPI bus, the /HOLD function can save the state of the instruction and the data in the buffer, so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, and not during Quad SPI or QPI. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as a /HOLD pin or a data I/O pin. When QE=0 (factory default), the pin is /HOLD. When QE=1, the pin will become an I/O pin, and the /HOLD function is no longer available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low, the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low, the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.1.7 Software Reset

The W25Q12PW can be reset to the initial power-on state by a software Reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30 μ s (t_{RST}) to reset.

The device /HOLD or /RESET (IO3) pin can also be configured to utilize a hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for the /HOLD pin function or the RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Driving the /RESET pin low for a minimum period of ~1 μ s (t_{RESET}^*) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted, and data corruption may happen. While /RESET is low, the device will not accept any command input.

If the QE bit is set to 1, the /HOLD or /RESET function will be disabled, and the pin will become one of the four data I/O pins.



6.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q12PW provides several means to protect the data from inadvertent writes.

6.2.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Registers
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

* Note: This feature is available upon special flow. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q12PW will maintain a reset condition while VCC is below the threshold value of V_{WI} , (See Power-up Timing and Voltage Levels and Figure 65). While reset, all operations are disabled, and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI} , all program and erase related instructions are further disabled for a time delay of t_{PUW} . This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resistor on /CS can be used to accomplish this.

After power-up, the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction, the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, SEC, TB, BP[2:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.



6.3 ECC Operation

Error Correction Code (ECC) is a commonly used technique in non-volatile memory to reduce the device Bit Error Rate (BER) during the device lifetime operation and to improve device reliability. To achieve error detection and correction, redundancy data must be added to store the ECC calculation results for a given length of data. In the W25Q12PW, the ECC calculation is done per aligned 16-byte memory address range partition (LSB A[3:0] = 0000b to 1111b) from the lowest address (00000000h) to the highest memory address (03FFFFFFh). Every byte up to the 16th byte of memory data being programmed in the aligned 16-byte memory address array is checked by the internal ECC engine using Single Error Correction (SEC). Using 16-Byte ECC data granularity, ECC calculation latency time is minimized, while preserving the highest level of data integrity.

The W25Q12PW device has an ECC register, the ECC Status Register a, which controls the ECC settings and monitors the ECC event. The ECC Status Register has Single Error Correction (SEC), and ECC On/Off (ECCO) bits to monitor the ECC events.

The default value of all memory data is FFh (Erased) when the device is shipped from the factory. A “Page Program (02h or 12h)” or a “Quad Page Program (32h or 34h)” command can be used to program the user data into the memory array. ECC calculation is performed during the internal programming operation, and the results are stored in the redundancy or spare area of the memory array. Error correction codes are calculated and stored based per 16-byte aligned address boundaries from LSB address A[3:0] = 0000b to 1111b and applicable across the full memory. Programming over previously programmed data is also tracked and monitored per aligned 16-byte memory. Every aligned 16-byte memory should be only programmed once with one byte up to 16 bytes of data, so ECC functionality (ECC On status or flag) will be maintained. If any of the aligned 16-byte memory is programmed more than once, the ECC functionality of those affected (targeted) 16-byte aligned memories will automatically be turned off (ECC Off status or flag) on read operations. Programming more than once on the same location from a single bit alteration up to the aligned 16-byte segment is accepted except the ECC functionality will automatically be turned off (ECC Off status or flag) during memory reads. ECC On/Off status is shown by ECC On/Off (ECCO) status bit of the ECC Status Register.

When ECC is active on an aligned 16-byte memory, read memory access to this address location is performed with the aid of the internal ECC engine which will check the ECC results stored in the spare area and apply the necessary error correction or error detection to the memory array data being read out. The Single Error Correction (SEC) Bit in the ECC Status Register provides ECC status after the last Read operation to determine if the data read out has any errors or not. A Read operation can start from any byte address and continue through the entire memory array. It is not necessary to align the 16-Byte granularity boundary address to start a Read command. When ECC is inactive (disabled) on an aligned 16-byte memory, during read memory operations, read access will be directly to the memory array location without any internal ECC check for error correction or detection. Please contact Winbond for an Application Note.

7. STATUS AND CONFIGURATION REGISTERS

W25Q12PW-DTR



The W25Q12PW has three Status and Configuration Registers. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, and power-up. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, Hold/Reset functions, and output driver strength. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

7.1 Status Registers

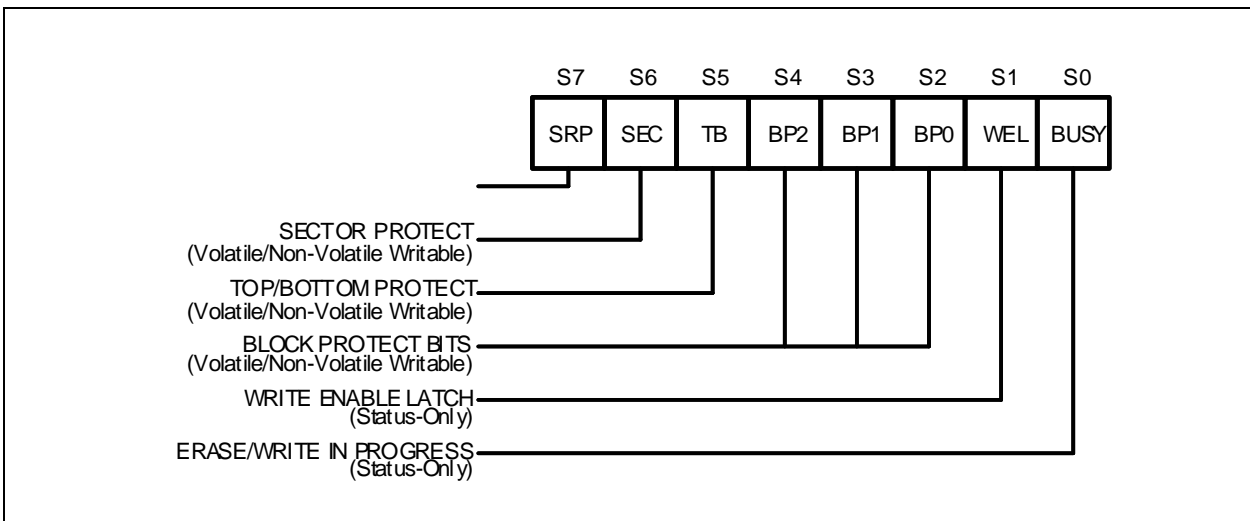


Figure 4a. Status Register-1

7.1.1 Erase/Write In Progress (BUSY) – Status Only

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time, the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see *tw*, *tPP*, *tSE*, *tBE*, and *tCE* in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating that the device is ready for further instructions.

7.1.2 Write Enable Latch (WEL) – Status Only

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.



7.1.3 Block Protect Bits (BP2, BP1, BP0) – Volatile/Non-Volatile Writable

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see *tw* in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, and none of the array is protected.

7.1.4 Top/Bottom Block Protect (TB) – Volatile/Non-Volatile Writable

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP, SRL and WEL bits.

7.1.5 Sector/Block Protect Bit (SEC) – Volatile/Non-Volatile Writable

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

7.1.6 Complement Protect (CMP) – Volatile/Non-Volatile Writable

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.



7.1.7 Status Register Protect (SRP, SRL)

The Status Register Protect bits (SRP) are non-volatile read/write bits in the status register (S7). The SRP bit controls the method of write protection: software protection or hardware protection. The Status Register Lock bits (SRL) are non-volatile/volatile read/write bits in the status register (S8). The SRL bit controls the method of write protection: temporary lock-down or permanently one time program.

SRL	SRP	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	X	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle. ⁽¹⁾
1	X	X	One Time Program ⁽²⁾	Status Register is permanently protected and cannot be written to. (enabled by adding prefix command AAh, 55h)

Note:

1. When SRL =1, a power-down, power-up cycle will change SRL =0 state.
2. Please contact Winbond for details regarding the special instruction sequence

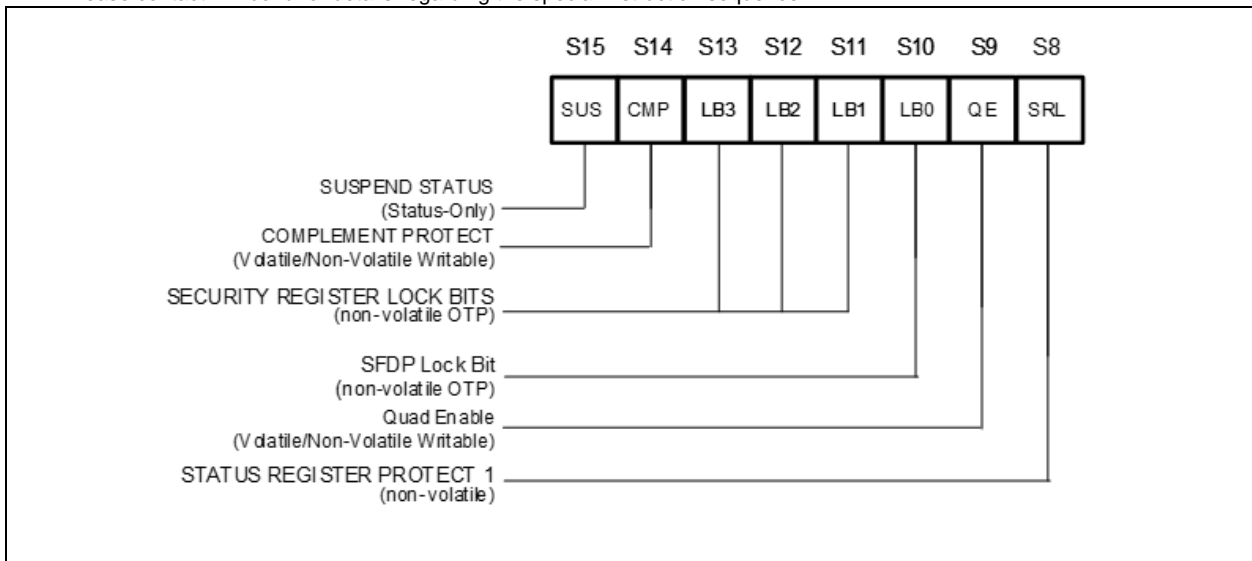


Figure 4b. Status Register-2



7.1.8 Erase/Program Suspend Status (SUS) – Status Only

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

7.1.9 Security Register Lock Bits (LB3, LB2, LB1, LB0) –Non-Volatile OTP Writable

The Security Register Lock Bits (LB3, LB2, LB1, LB0) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11, S10) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-0 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

The default state of LB0 is 1, SFDP Register is locked.

7.1.10 Quad Enable (QE) – Volatile/Non-Volatile Writable

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options “IM” & “JM”), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1(factory default for Quad Enabled part numbers with ordering option “IQ” & “JQ”), the Quad IO2 and IO3 pins are enabled, and the /WP and the /HOLD functions are disabled.

The QE bit is required to be set to a 1 before issuing an “Enter QPI (38h)” to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command will be ignored. When the device is in QPI mode, the QE bit will remain to be a 1. A “Write Status Register” command in QPI mode cannot change the QE bit from a “1” to a “0”.

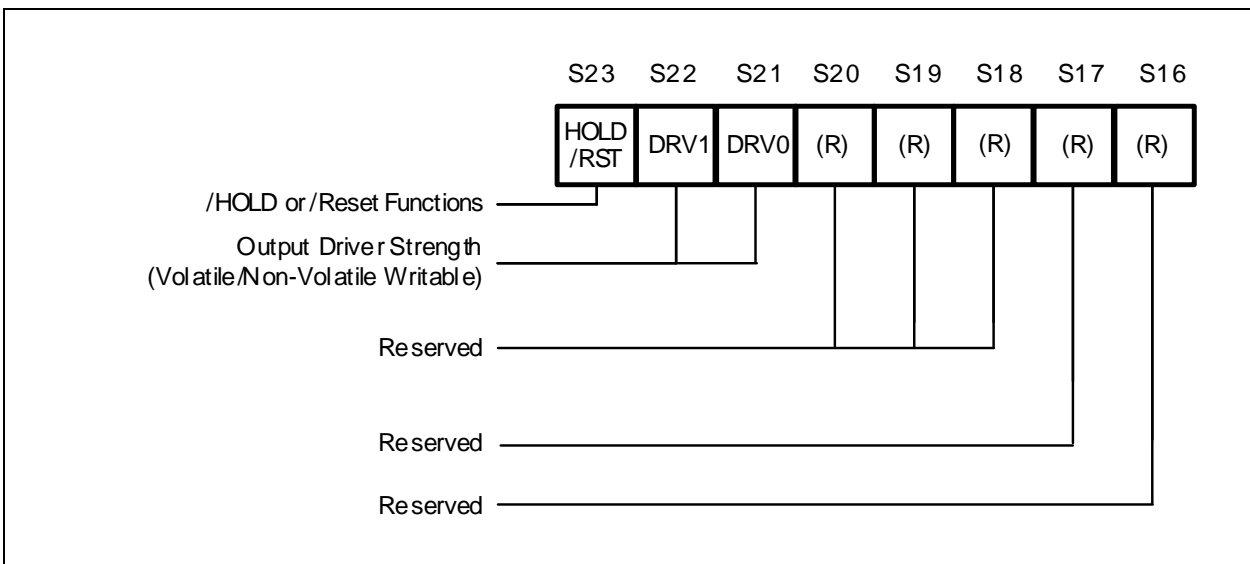


Figure 4c. Status Register-3



7.1.11 Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Resistor
0, 0	25-ohm
0, 1	33-ohm
1, 0	50-ohm(default)
1, 1	100-ohm

7.1.12 /HOLD or /RESET Pin Function (HOLD/RST) – Volatile/Non-Volatile Writable

The HOLD/RST bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

7.1.13 Reserved Bits – Non Functional

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effect.

W25Q12PW-DTR



7.1.14 W25Q12PW Status Register Memory Protection (CMP = 0)

STATUS REGISTER ⁽¹⁾					W25Q12PW (128M-BIT) MEMORY PROTECTION ⁽³⁾			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION ⁽²⁾
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 thru 255	FC0000h – FFFFFFFh	256KB	Upper 1/64
0	0	0	1	0	248 thru 255	F80000h – FFFFFFFh	512KB	Upper 1/32
0	0	0	1	1	240 thru 255	F00000h – FFFFFFFh	1MB	Upper 1/16
0	0	1	0	0	224 thru 255	E00000h – FFFFFFFh	2MB	Upper 1/8
0	0	1	0	1	192 thru 255	C00000h – FFFFFFFh	4MB	Upper 1/4
0	0	1	1	0	128 thru 255	800000h – FFFFFFFh	8MB	Upper 1/2
0	1	0	0	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/64
0	1	0	1	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/32
0	1	0	1	1	0 thru 15	000000h – 0FFFFFFh	1MB	Lower 1/16
0	1	1	0	0	0 thru 31	000000h – 1FFFFFFh	2MB	Lower 1/8
0	1	1	0	1	0 thru 63	000000h – 3FFFFFFh	4MB	Lower 1/4
0	1	1	1	0	0 thru 127	000000h – 7FFFFFFh	8MB	Lower 1/2
X	X	1	1	1	0 thru 255	000000h – FFFFFFFh	16MB	ALL
1	0	0	0	1	255	FFF000h – FFFFFFFh	4KB	U - 1/4096
1	0	0	1	0	255	FFE000h – FFFFFFFh	8KB	U - 1/2048
1	0	0	1	1	255	FFC000h – FFFFFFFh	16KB	U - 1/1024
1	0	1	0	X	255	FF8000h – FFFFFFFh	32KB	U - 1/512
1	1	0	0	1	0	000000h – 000FFFh	4KB	L - 1/4096
1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/2048
1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/1024
1	1	1	0	X	0	000000h – 007FFFh	32KB	L - 1/512

Notes:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

W25Q12PW-DTR



7.1.15 W25Q12PW Status Register Memory Protection (CMP = 1)

STATUS REGISTER ⁽¹⁾					W25Q12PW (128M-BIT) MEMORY PROTECTION ⁽³⁾			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION ⁽²⁾
X	X	0	0	0	0 thru 255	000000h - FFFFFFFh	16MB	ALL
0	0	0	0	1	0 thru 251	000000h - FBFFFFh	16,128KB	Lower 63/64
0	0	0	1	0	0 thru 247	000000h - F7FFFFh	15,872KB	Lower 31/32
0	0	0	1	1	0 thru 239	000000h - EFFFFFFh	15MB	Lower 15/16
0	0	1	0	0	0 thru 223	000000h - DFFFFFFh	14MB	Lower 7/8
0	0	1	0	1	0 thru 191	000000h - BFFFFFFh	12MB	Lower 3/4
0	0	1	1	0	0 thru 127	000000h - 7FFFFFFh	8MB	Lower 1/2
0	1	0	0	1	4 thru 255	040000h - FFFFFFFh	16,128KB	Upper 63/64
0	1	0	1	0	8 thru 255	080000h - FFFFFFFh	15,872KB	Upper 31/32
0	1	0	1	1	16 thru 255	100000h - FFFFFFFh	15MB	Upper 15/16
0	1	1	0	0	32 thru 255	200000h - FFFFFFFh	14MB	Upper 7/8
0	1	1	0	1	64 thru 255	400000h - FFFFFFFh	12MB	Upper 3/4
0	1	1	1	0	128 thru 255	800000h - FFFFFFFh	8MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 255	000000h - FFEFFFFh	16,380KB	L - 4095/4096
1	0	0	1	0	0 thru 255	000000h - FFDFFFFh	16,376KB	L - 2047/2048
1	0	0	1	1	0 thru 255	000000h - FFBFFFFh	16,368KB	L - 1023/1024
1	0	1	0	X	0 thru 255	000000h - FF7FFFFh	16,352KB	L - 511/512
1	1	0	0	1	0 thru 255	001000h - FFFFFFFh	16,380KB	U - 4095/4096
1	1	0	1	0	0 thru 255	002000h - FFFFFFFh	16,376KB	U - 2047/2048
1	1	0	1	1	0 thru 255	004000h - FFFFFFFh	16,368KB	U - 1023/1024
1	1	1	0	X	0 thru 255	008000h - FFFFFFFh	16,352KB	U - 511/512

Notes:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.



7.2 Error Code Correction (ECC) Registers

7.2.1 ECC Status Register – Volatile Writable and Readable

The W25Q12PW provides a volatile ECC Status Register which consists of the configuration bits for advanced features for error correction, and flash memory cell abnormality detection. Upon power up or after the execution of a Software Reset, the ECC Status Register bits will be reset to their default value – SEC and ECCO bits default value is 0 and ECC bit default value is 1.

The remaining ECC Register bits namely Single Error Correction bit (ER7), and ECC On/Off bit (ER0) are read status only bits. The Read ECC Status Register instruction (25h) is used to read the ECC Status Register.

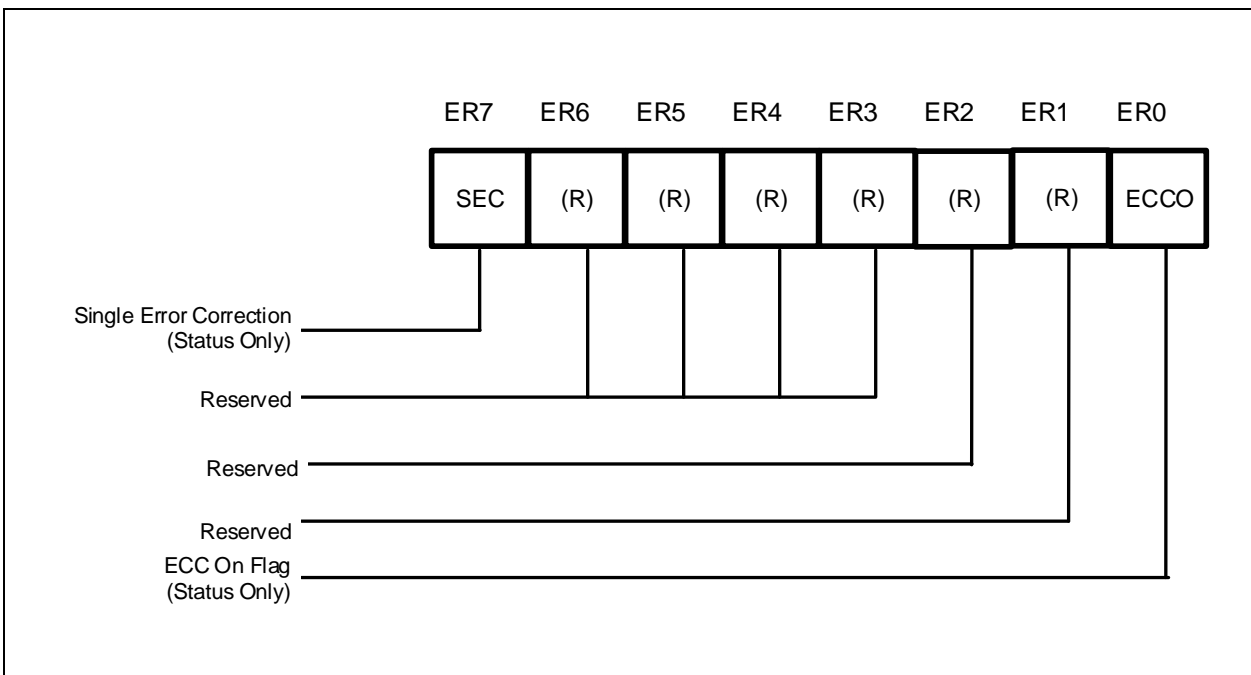


Figure 5f. ECC Status Register



7.2.1.1. ECC Status Bits (SEC) – Status Only

The SEC (Single Error Correction) Status Bit is used to show the ECC results for the last Read operation. The SEC bit will be cleared to 0 once the device accepts a new Read command.

SEC	Definitions
0	No ECC events in all aligned 16-Byte granularities.
1	SEC events in single or multiple 16-Byte granularities, data is OK to use (unless it's odd bits error in 16-Byte granularity).

7.2.1.2. ECC On/Off (ECCO) – Status Only

The ECC On/Off bit is a status indicator if the ECC function is active or inactive (disabled) on any of the 16-byte aligned memory from the last memory read operation. When the ECC On/Off bit is '0' (default), the ECC function is active in all the 16-byte aligned memory from the last memory read operation. When ECC On/Off bit is '1', the ECC function has been turned off (disabled) in one of the 16-byte aligned memory from the last memory read operation. The ECC On/Off bit is automatically turned off (disabled) if any of the aligned 16-byte memory address ranges are programmed more than once before an erase operation.



7.3. Page Buffer

In Standard SPI mode, one of the new powerful features of the W25Q12PW is the integrated Serial SRAM buffer and its associated Program Buffer. Together, the 256-byte Serial SRAM provides usable SRAM storage. The SRAM can be used in conjunction with the Flash memory or independently. The main purpose of the Serial SRAM is to serve as the primary buffer for data to be written into the Serial Flash memory array. In case of need, it can help to transform random Byte Writes to page Program Buffer.

Using the Write Buffer instruction, data is first shifted into the SRAM from the SPI bus. When the instruction sequence has been completed, the entire 256-bytes is transferred to the Program Buffer. The Program Buffer supports the array during the Erase/Write cycle (tWP), freeing the SRAM to accept new data. This double-buffering scheme increases erase/write transfer rates and can eliminate the need for external RAM buffers (Figure 4e). The SRAM is fully byte-addressable. Thus, the entire 256-bytes, a single byte, or a sequence of bytes can be read from or written to the SRAM. This allows the SRAM to be used as a temporary work area for read-modify-write operations prior to a sector write.

The Transfer Sector to SRAM instruction allows the contents of a specified sector of Flash memory to be moved to the SRAM. This can be useful when only a portion of a sector needs to be altered. In this case, the sector is first transferred to the SRAM, where modifications are made using the Write to SRAM instruction. Once complete, a Transfer SRAM to Sector instruction is used to update the sector.

Page Buffer control instruction as below:

- Clear Buffer(81h): Reset all the bit in the Page Buffer becomes '1'.
- Write Buffer(82h): Write the data into the Page Buffer, from the 1st byte to the 256th byte.
- Read Buffer(83h): Read out the data from Page Buffer.
- Program Buffer(8Ah): Write the Page Buffer data into the specified Flash Physical memory page.
- Load Buffer(8Bh): Read the data from the specified Flash Physical memory page into the Page Buffer.

Upon power off or the execution of a reset, all bits in the Page Buffer become '1', effectively clearing the buffer. After Release Power-down(ABh), a clear buffer command must be issued."

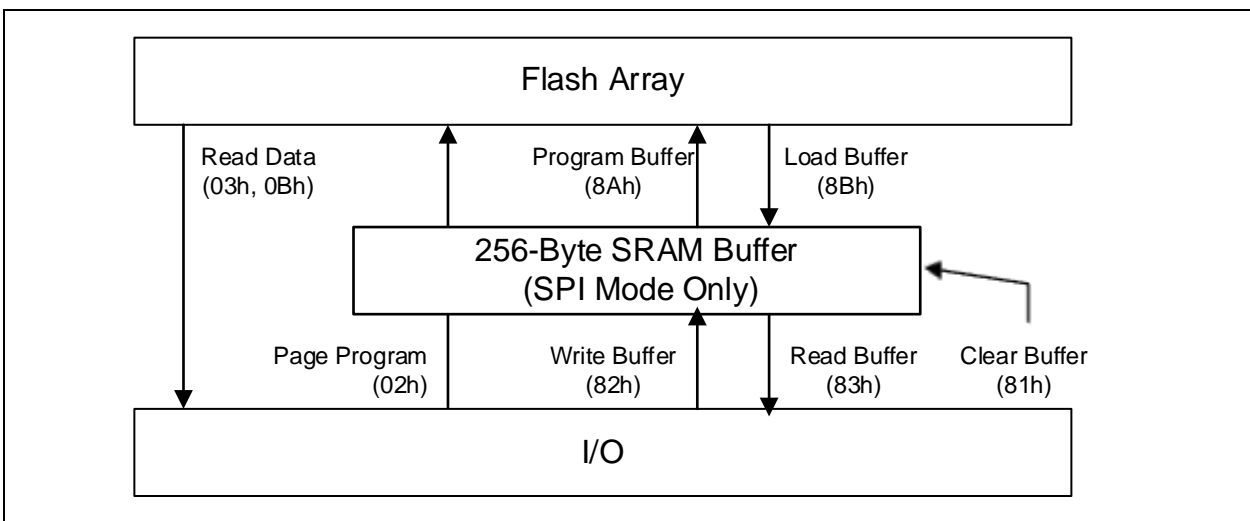


Figure 4e. Serial Flash Buffer Mode
For details, please refer to the application note on 'Winbond SPI NOR Flash Page Buffer Operation'



8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25Q12PW consists of 47 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1-2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI instruction set of the W25Q12PW consists of 36 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table 3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked through IO[3:0] pins provides the instruction code. Data on all four IO pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI instructions, addresses, data and dummy byte use all four IO pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of /CS. Clock relative timing diagrams for each instruction are included in Figures 5 through 57. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.1 Device ID and Instruction Set Tables

8.1.1 Manufacturer and Device Identification

MANUFACTURER ID	(MF7 - MF0)	
Winbond Serial Flash	EFh	
Device ID	(ID7 - ID0)	(ID15 - ID0)
Instruction	ABh, 90h, 92h, 94h	9Fh
W25Q128PW-IM	17h	8018h

W25Q12PW-DTR



Instruction Set Table 1 (Standard SPI Instructions)⁽¹⁾

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock₍₁₋₁₋₁₎	8	8	8	8	8	8	8
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Release Power-down	ABh						
Read ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0) ⁽²⁾		
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read Unique ID	4Bh	Dummy	Dummy	Dummy	Dummy	(UID63-0)	
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)		
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0 ⁽³⁾	
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Read Status Register-1	05h	(S7-S0) ⁽²⁾					
Write Status Register-1	01h	(S7-S0)					
Read Status Register-2	35h	(S15-S8) ⁽²⁾					
Write Status Register-2	31h	(S15-S8)					
Read Status Register-3	15h	(S23-S16) ⁽²⁾					
Write Status Register-3	11h	(S23-S16)					
Read ECC Status Register	25h	(ER7-ER0) ⁽²⁾					
Read SFDP Register	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase Security Register ⁽⁴⁾	44h	A23-A16	A15-A8	A7-A0			
Program Security Register ⁽⁴⁾	42h	A23-A16	A15-A8	A7-A0	D7-D0 ⁽³⁾		
Read Security Register ⁽⁴⁾	48h	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase / Program Suspend	75h						
Erase / Program Resume	7Ah						
Power-down	B9h						
Set Read Parameters	C0h	P7-P0					
Enter QPI Mode	38h						
Enable Reset	66h						
Reset Device	99h						
Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock₍₁₋₁₋₁₎	8	8	8	8	8	8	8
Clear Buffer	81h	A23-A16	A15-A8	A7-A0			
Write Buffer	82h	A23-A16	A15-A8	A7-A0	D7-D0	...	
Read Buffer	83h	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Program Buffer	8Ah	A23-A16	A15-A8	A7-A0			
Load Buffer	8Bh	A23-A16	A15-A8	A7-A0			

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8.1.2 Instruction Set Table 2 (Dual/Quad SPI Instructions)⁽¹⁾

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Number of Clock ₍₁₋₁₋₂₎	8	8	8	8	4	4	4	4	4
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0) ⁽⁶⁾	...	
Number of Clock ₍₁₋₂₋₂₎	8	4	4	4	4	4	4	4	4
Fast Read Dual I/O	BBh	A23-A16 ⁽⁵⁾	A15-A8 ⁽⁵⁾	A7-A0 ⁽⁵⁾	M7-M0	(D7-D0) ⁽⁶⁾	...		
Mftr./Device ID Dual I/O	92h	A23-A16 ⁽⁵⁾	A15-A8 ⁽⁵⁾	00 ⁽⁵⁾	Dummy ⁽¹⁷⁾	(MF7-MF0) ₍₆₎	(ID7-ID0) ⁽⁶⁾		
Number of Clock ₍₁₋₁₋₄₎	8	8	8	8	2	2	2	2	2
Quad Input Page Program	32h	A23-A16	A15-A8	A7-A0	(D7-D0) ⁽⁸⁾	(D7-D0) ⁽³⁾	...		
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0) ⁽⁹⁾
Number of Clock ₍₁₋₄₋₄₎	8	2 ⁽⁷⁾	2 ⁽⁷⁾	2 ⁽⁷⁾	2	2	2	2	2
Mftr./Device ID Quad I/O	94h	A23-A16	A15-A8	00	Dummy ⁽¹³⁾	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0 ⁽¹³⁾	Dummy ⁽¹¹⁾	Dummy ⁽¹¹⁾	(D7-D0)	...
Set Burst with Wrap	77h	Dummy	Dummy	Dummy	W7-W0				

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8.1.3 Instruction Set Table 3 (QPI Instructions)⁽¹⁰⁾

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (4-4-4)	2	2	2	2	2	2	2
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Release Power-down	ABh						
Read ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0) ⁽²⁾		
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Set Read Parameters	C0h	P7-P0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0 ⁽⁹⁾	D7-D0 ⁽³⁾	...
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Read Status Register-1	05h	(S7-S0) ⁽²⁾					
Write Status Register-1	01h	(S7-S0)					
Read Status Register-2	35h	(S15-S8) ⁽²⁾					
Write Status Register-2	31h	(S15-S8)					
Read Status Register-3	15h	(S23-S16) ⁽²⁾					
Write Status Register-3	11h	(S23-S16)					
Read ECC Status Register	25h	(ER7-ER0) ⁽²⁾					
Erase / Program Suspend	75h						
Erase / Program Resume	7Ah						
Power-down	B9h						
Enable Reset	66h						
Reset Device	99h						
Exit QPI Mode	FFh						
Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (4-4-4)	2	2	2	2	2	4	2
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	Dummy ⁽¹¹⁾	(D7-D0)
Burst Read with Wrap	0Ch	A23-A16	A15-A8	A7-A0	Dummy ⁽¹²⁾	Dummy ⁽¹¹⁾	(D7-D0)
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0 ⁽¹⁴⁾	Dummy ⁽¹¹⁾	(D7-D0)
Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5-Byte 8		Byte 9
Number of Clock (4-4-4)	2	2	2	2	2-2-2-2		2
Read SFDP Register	5Ah	A23-A16	A15-A8	A7-A0	Dummy		(D7-D0)...

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8.1.4 Instruction Set Table 4 (DTR with SPI Instructions)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (1-1d-1d)	8	4	4	4	6	4	4
DTR Fast Read	0Dh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	...
Number of Clock (1-2d-2d)	8	2	2	2	6	2	2
DTR Fast Read Dual I/O	BDh	A23-A16	A15-A8	A7-A0	Dummy ⁽¹⁴⁾	(D7-D0)
Number of Clock (1-4d-4d)	8	1	1	1	8	1	1
DTR Fast Read Quad I/O ⁽¹⁴⁾	EDh	A23-A16	A15-A8	A7-A0	Dummy ^(12, 14)	(D7-D0)	(D7-D0)

8.1.5 Instruction Set Table 5 (DTR with QPI Instructions)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (4-4d-4d)	2	1	1	1	8	1	1
DTR Burst Read with Wrap ⁽¹³⁾	0Eh	A23-A16	A15-A8	A7-A0	Dummy ⁽¹¹⁾	(D7-D0)	...
DTR Fast Read	0Dh	A23-A16	A15-A8	A7-A0	Dummy ⁽¹¹⁾	(D7-D0)	...
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	Dummy ^(11, 14)	(D7-D0)	



Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “()” indicate data output from the device on either 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Security Register Address:
 Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
 Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
 Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address
5. Dual SPI address input format:
 IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
 IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
6. Dual SPI data output format:
 IO0 = (D6, D4, D2, D0)
 IO1 = (D7, D5, D3, D1)
7. Quad SPI address input format:
 IO0 = A20, A16, A12, A8, A4, A0, M4, M0
 IO1 = A21, A17, A13, A9, A5, A1, M5, M1
 IO2 = A22, A18, A14, A10, A6, A2, M6, M2
 IO3 = A23, A19, A15, A11, A7, A3, M7, M3
- Set Burst with Wrap input format:
 IO0 = x, x, x, x, x, x, W4, x
 IO1 = x, x, x, x, x, x, W5, x
 IO2 = x, x, x, x, x, x, W6, x
 IO3 = x, x, x, x, x, x, x, x
8. Quad SPI data input/output format:
 IO0 = (D4, D0,)
 IO1 = (D5, D1,)
 IO2 = (D6, D2,)
 IO3 = (D7, D3,)
9. Fast Read Quad I/O data output format:
 IO0 = (x, x, x, x, D4, D0, D4, D0)
 IO1 = (x, x, x, x, D5, D1, D5, D1)
 IO2 = (x, x, x, x, D6, D2, D6, D2)
 IO3 = (x, x, x, x, D7, D3, D7, D3)
10. QPI Command, Address, Data input/output format:

CLK #	0	1	2	3	4	5	6	7	8	9	10	11
IO0 =	C4, C0,	A20, A16,	A12, A8,	A4, A0,	D4, D0,	D4, D0						
IO1 =	C5, C1,	A21, A17,	A13, A9,	A5, A1,	D5, D1,	D5, D1						
IO2 =	C6, C2,	A22, A18,	A14, A10,	A6, A2,	D6, D2,	D6, D2						
IO3 =	C7, C3,	A23, A19,	A15, A11,	A7, A3,	D7, D3,	D7, D3						
11. The number of dummy clocks for QPI Fast Read, SPI/QPI Fast Read Quad I/O, & QPI Burst Read with Wrap is controlled by read parameter P6 – P4. The number of dummy clocks for SPI/QPI DTR Fast Read Quad I/O (EDh), QPI DTR Fast Read (0Dh), and DTR Burst Read with Wrap (0Eh) in QPI mode instructions is also controlled by the Read Parameter P6 – P4.
12. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P1 – P0.
13. “Set Burst Wrap (77h)” instruction controls enable/disable of wrap around and sets the wrap length.
14. The first dummy is the “Read Command Bypass Mode” bits M(7-0).



8.2 Instruction Descriptions

8.2.1 Write Enable (06h)

The Write Enable instruction (Figure 5) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

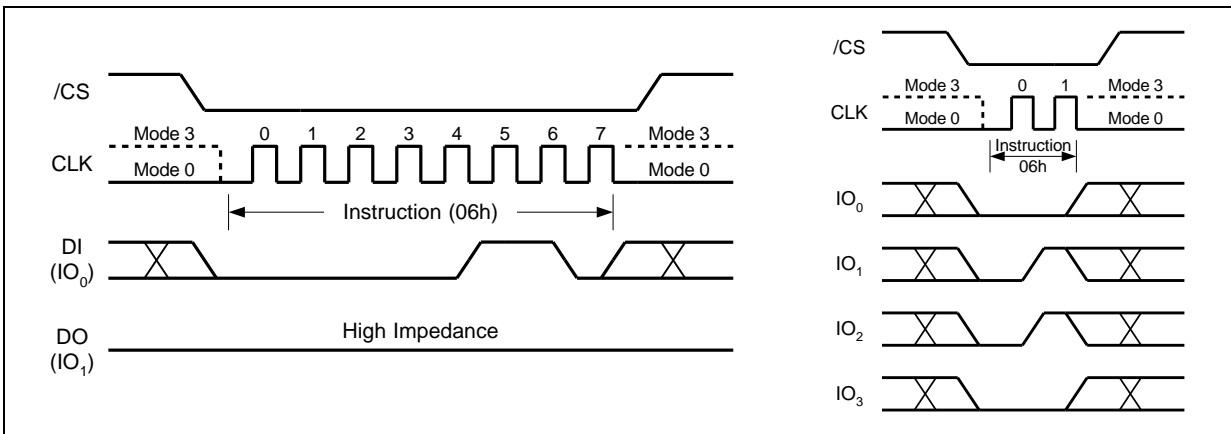


Figure 5. Write Enable Instruction for SPI Mode (left) or QPI Mode (right)



8.2.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 7.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h/31h/11h) instruction. The Write Enable for Volatile Status Register instruction (Figure 6) will not set the Write Enable Latch (WEL) bit. Only the Write Status Register instruction can change the volatile Status Register bit values.

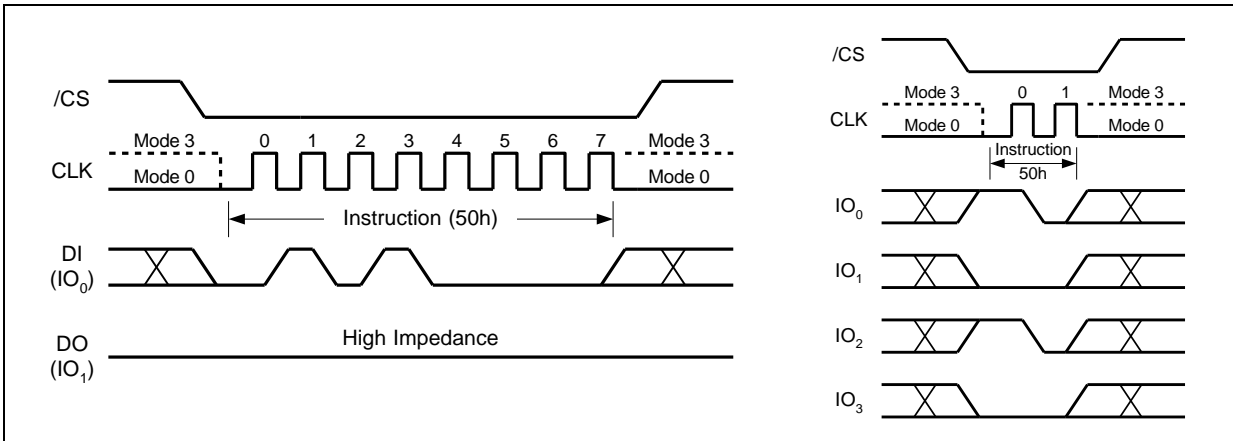


Figure 6. Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)

8.2.3 Write Disable (04h)

The Write Disable instruction (Figure 7) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

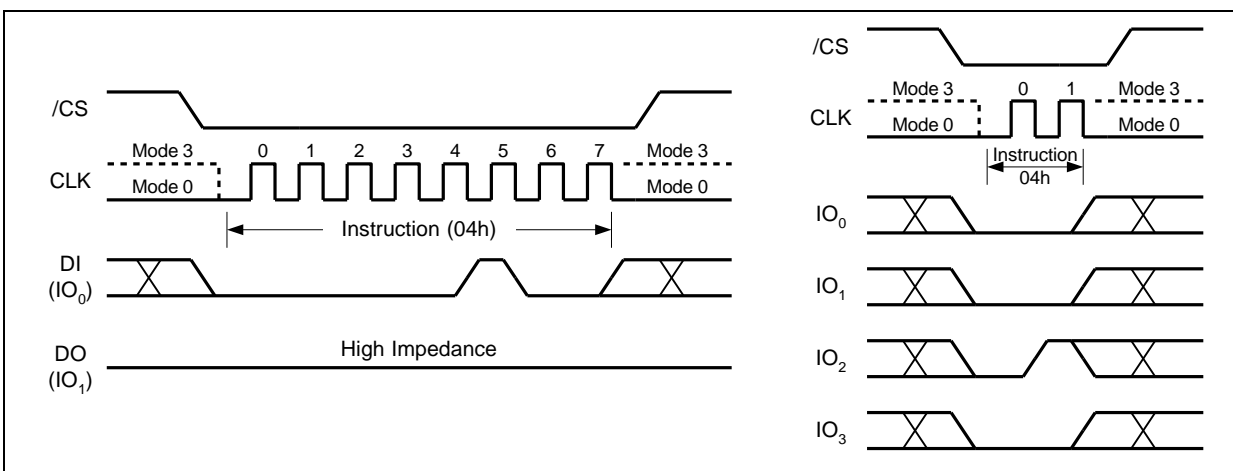


Figure 7. Write Disable Instruction for SPI Mode (left) or QPI Mode (right)



8.2.4 Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first as shown in Figure 8. Refer to section 7.1 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 8. The instruction is completed by driving /CS high.

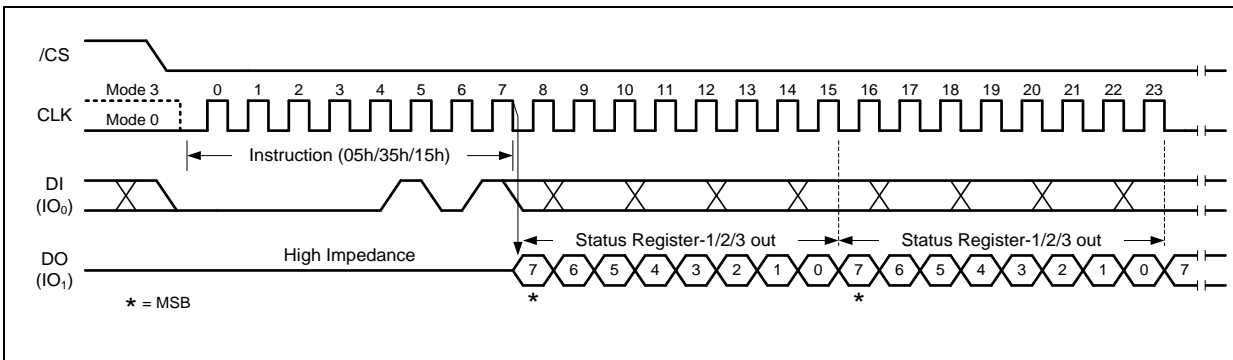


Figure 8a. Read Status Register Instruction (SPI Mode)

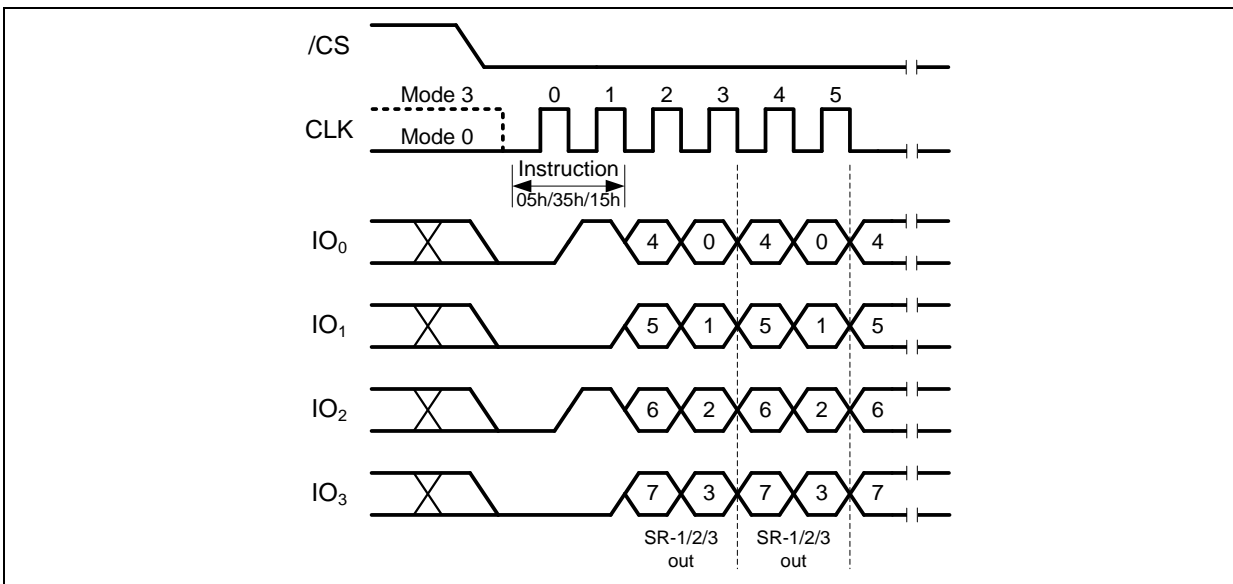


Figure 8b. Read Status Register Instruction (QPI Mode)



8.2.5 Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP, SEC, TB, BP[2:0] in Status Register-1; CMP, LB[3:1], QE, SRL in Status Register-2; HOLD/RST, DRV1, and DRV0 in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, and once the bits are set to 1, they cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code "01h/31h/11h", and then writing the status register data byte as illustrated in Figure 9a & 9b.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRL and LB[3:1] cannot be changed from "1" to "0" because of the OTP protection for these bits. Upon power off or the execution of a Software Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During a non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_w (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See AC Characteristics). The BUSY bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode. refer to section 7.1 for Status Register descriptions.

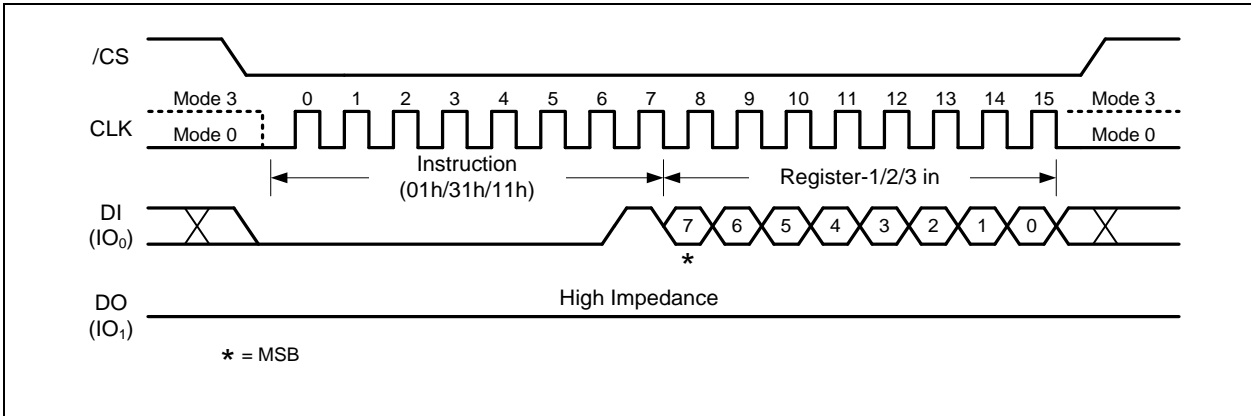


Figure 9a. Write Status Register-1/2/3 Instruction (SPI Mode)

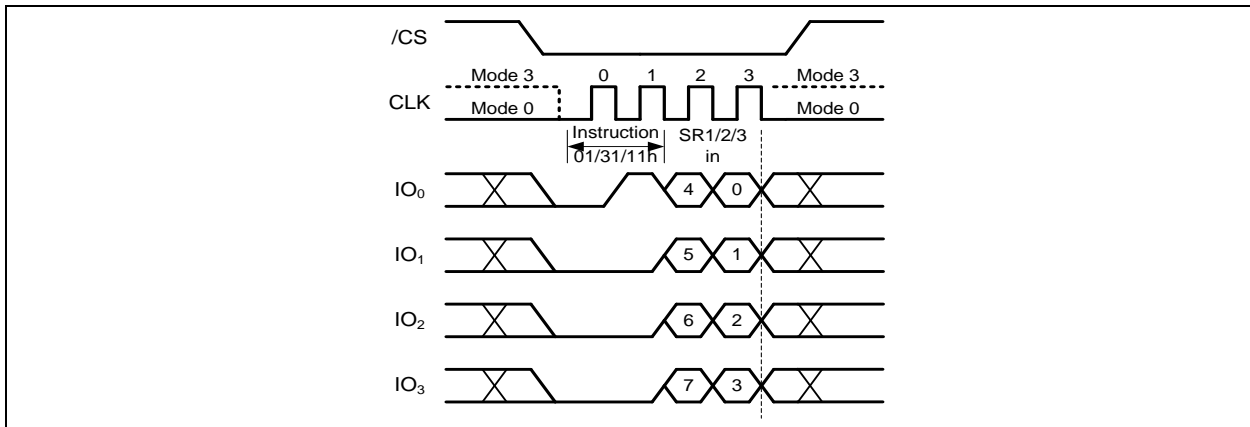


Figure 9b. Write Status Register-1/2/3 Instruction (QPI Mode)



8.2.6 Read ECC Status Register (25h)

ECC Status Register contains bits including SEC and ECC ON/OFF bits as described in Section 7.2.1. The Read ECC Status Register instruction is entered by driving /CS low and shifting the instruction code “25h” into the DI pin on the rising edge of CLK. The ECC Status Register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 11a. The Read ECC Status Register instruction in QPI mode sequence is shown on Figure 11b. Please contact Winbond for an Application Note.

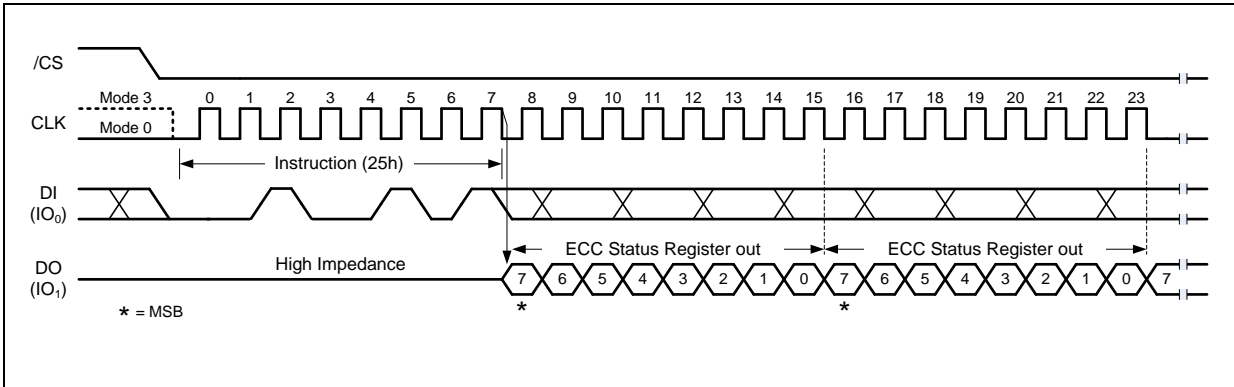


Figure 11a. Read ECC Status Register Instruction (SPI Mode)

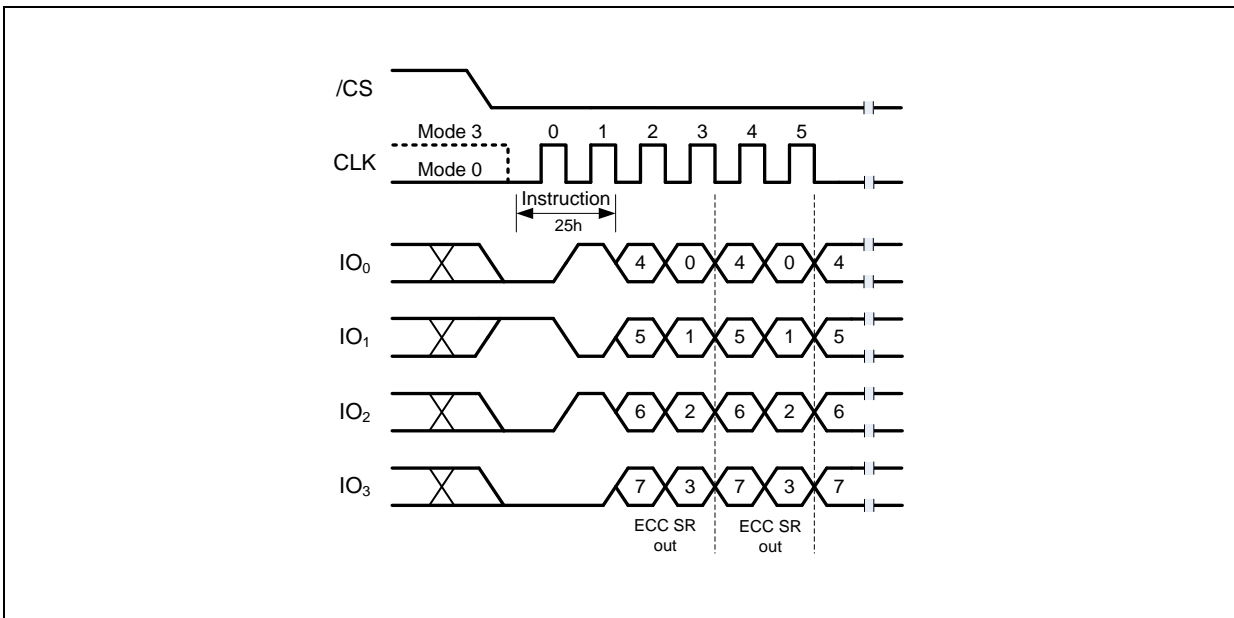


Figure 11b. Read ECC Status Register Instruction (QPI Mode)



8.2.7 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 14. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1), the instruction is ignored and will not have any effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Data (03h) instruction is only supported in Standard SPI mode.

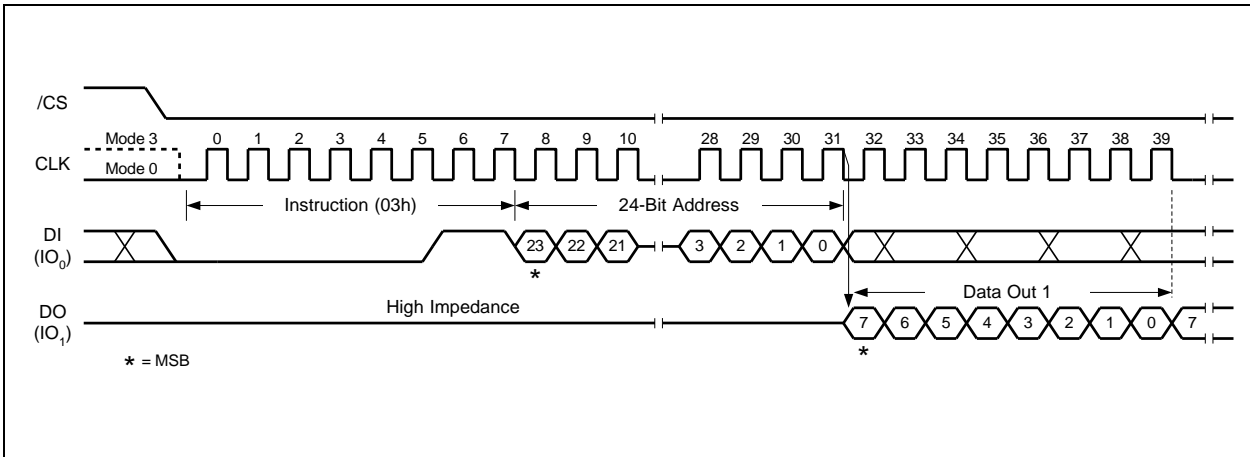


Figure 14. Read Data Instruction (SPI Mode only)



8.2.8 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 16. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the DO pin is a “don’t care”.

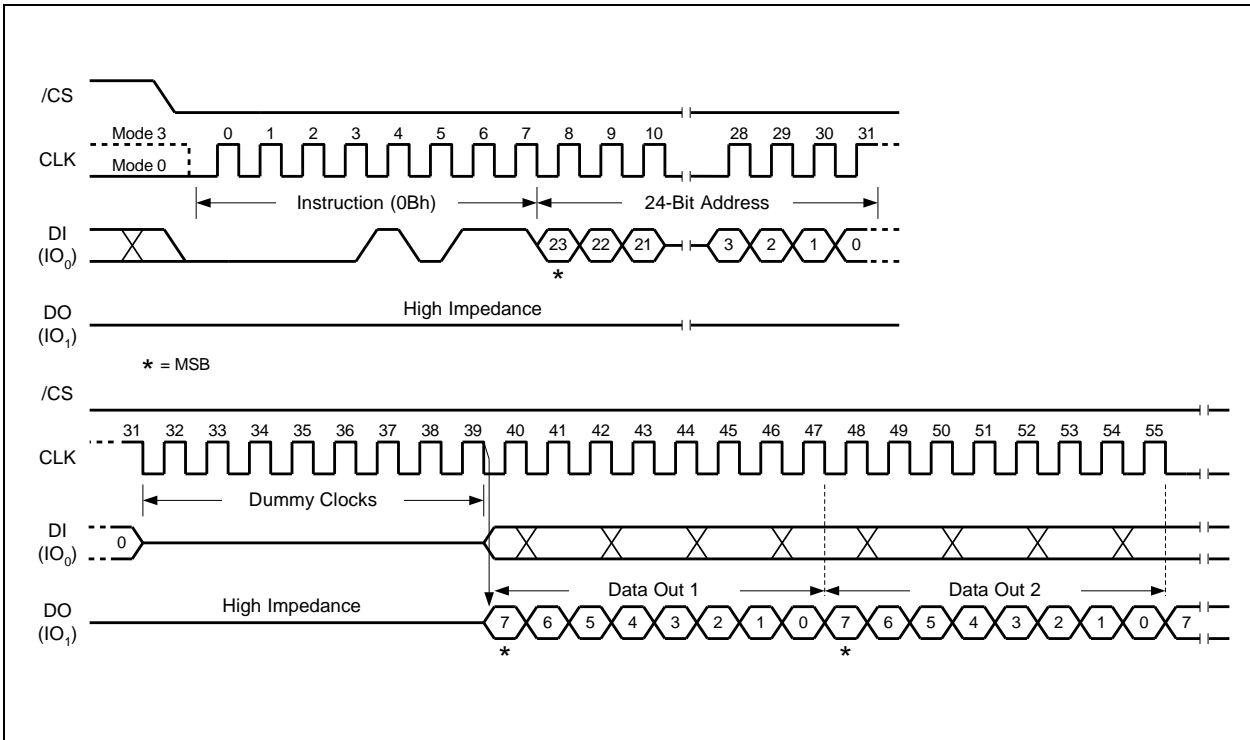


Figure 16a. Fast Read Instruction (SPI Mode)



Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured as either 6, 8, 10, 12 or 16. The default number of dummy clocks upon power up or after a Reset instruction is 6.

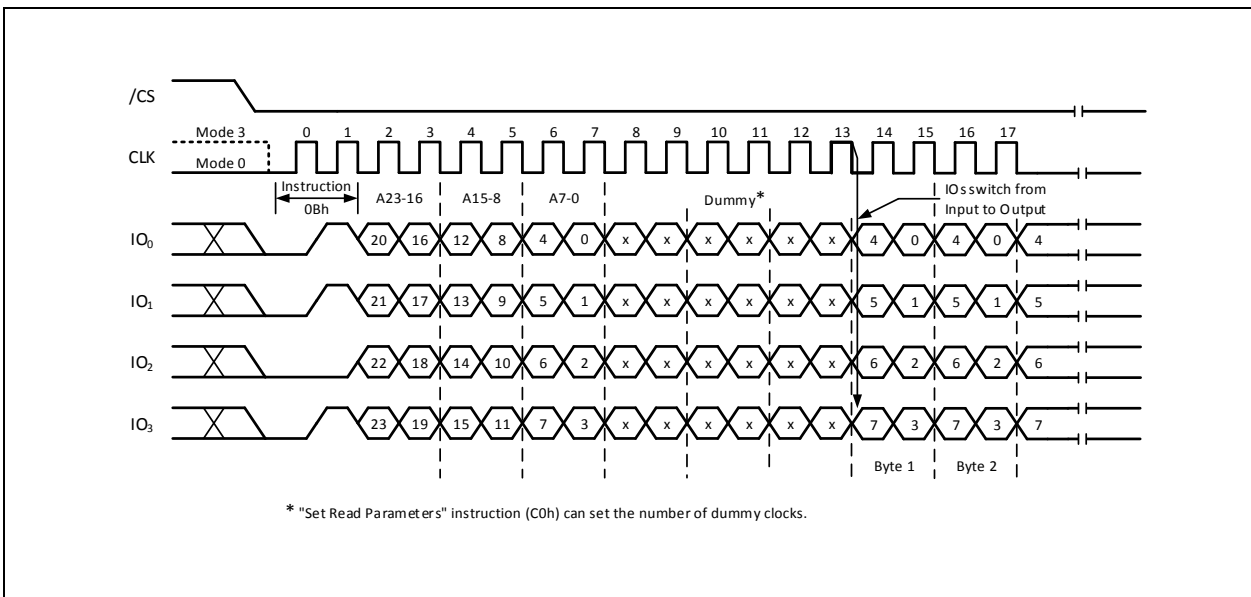


Figure 16b. Fast Read Instruction (QPI Mode)

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8.2.9 DTR Fast Read (0Dh)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24-bit address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding six “dummy” clocks after the 24-bit address as shown in Figure 17. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the DO pin is a “don’t care”.

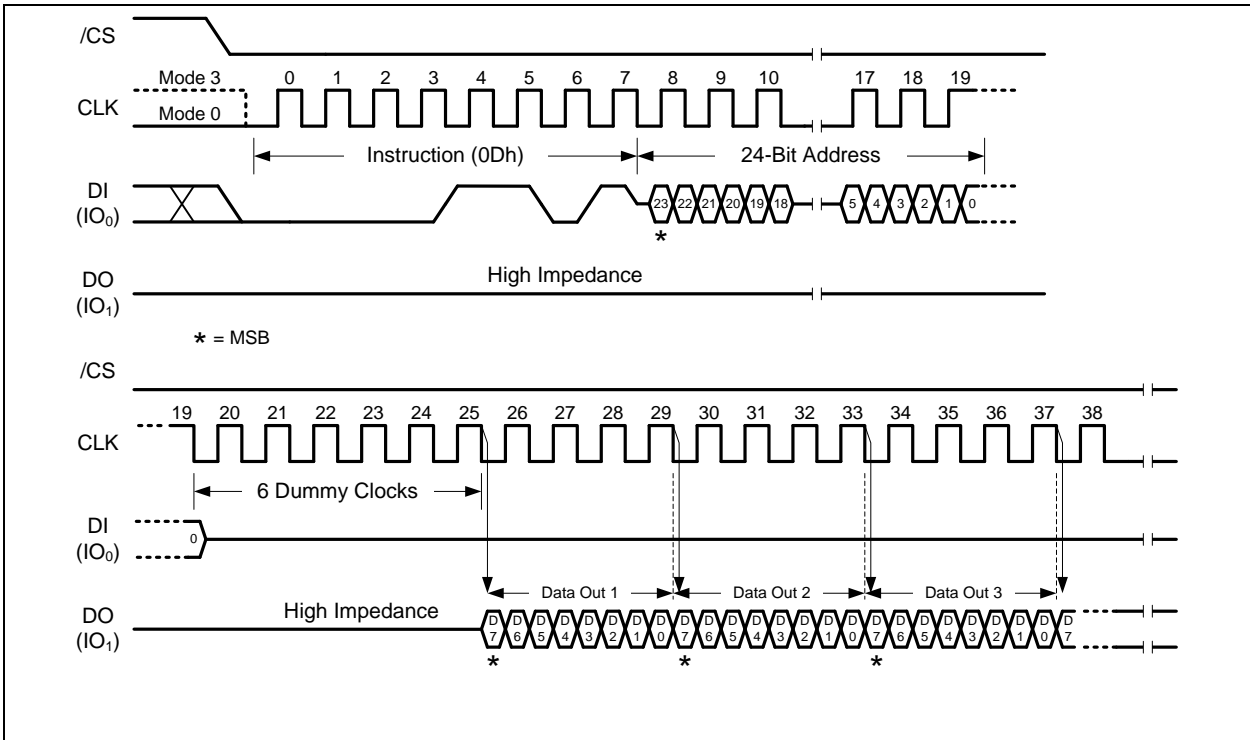


Figure 17a. DTR Fast Read Instruction (SPI Mode)

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DTR Fast Read (0Dh) in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode.

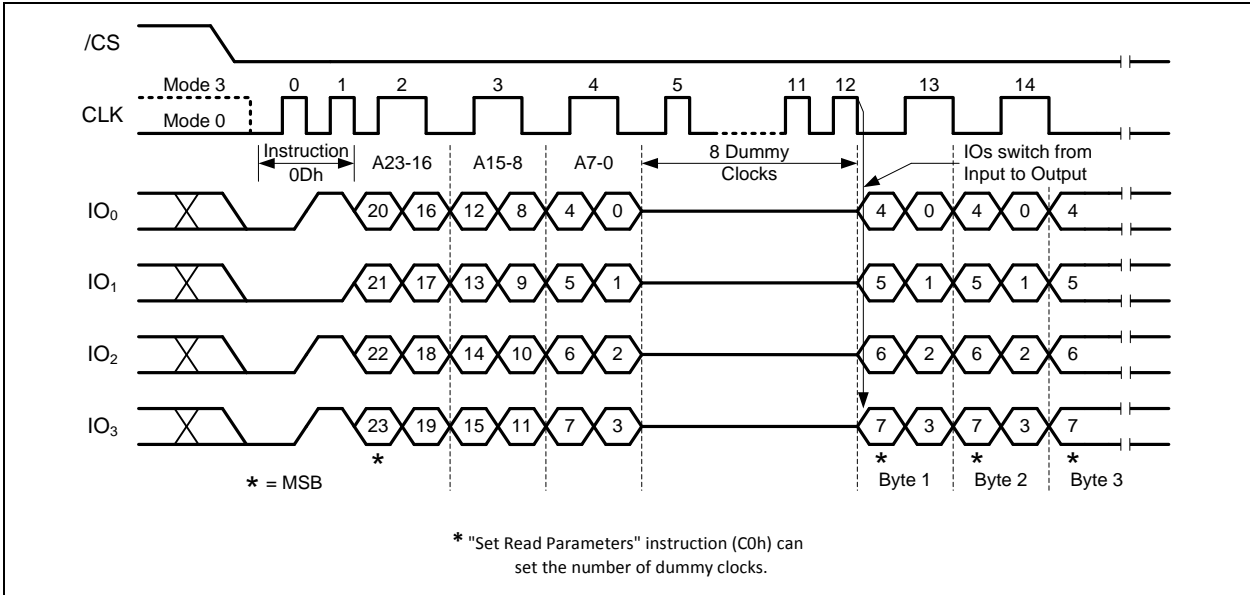


Figure 17b. DTR Fast Read Instruction (QPI Mode)



8.2.10 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO₀ and IO₁. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 18. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don't care”. However, the IO₀ pin should be high-impedance prior to the falling edge of the first data out clock.

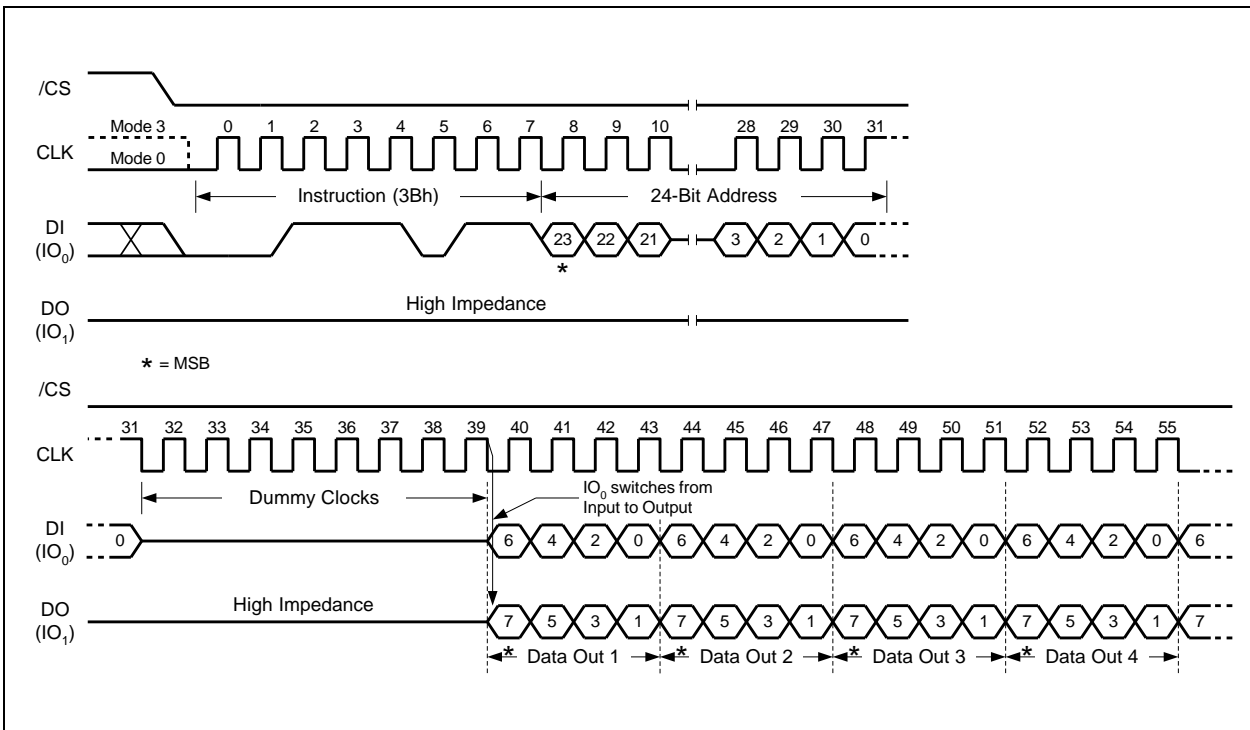


Figure 18. Fast Read Dual Output Instruction (SPI Mode only)



8.2.11 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO₀, IO₁, IO₂, and IO₃. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 20. The dummy clocks allow the device’s internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

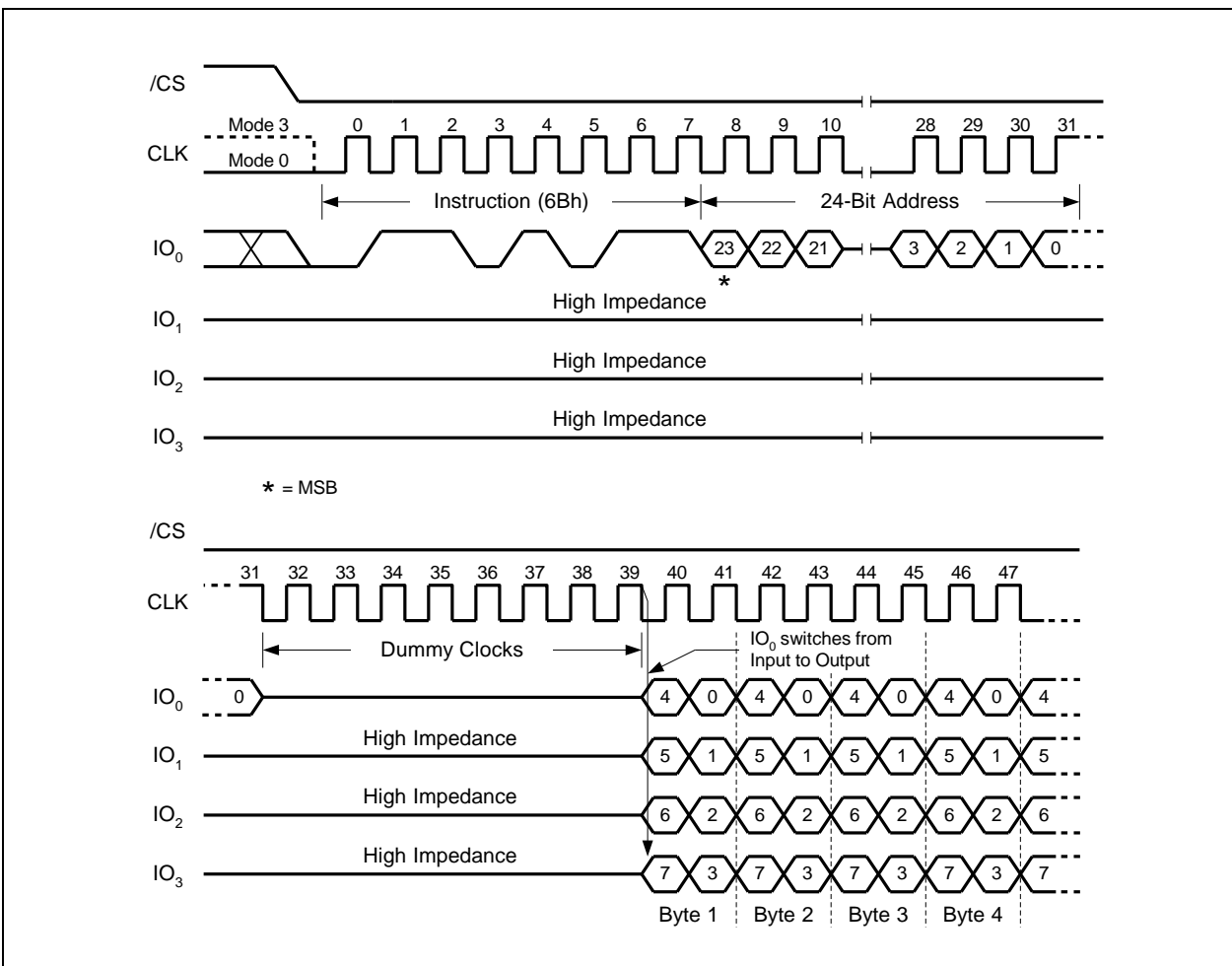


Figure 20. Fast Read Quad Output Instruction (SPI Mode only)



8.2.12 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO₀ and IO₁. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with “Read Command Bypass Mode”

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the “Read Command Bypass Mode” bits (M7-0) after the input Address bits (A23-0), as shown in Figure 22a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the “Read Command Bypass Mode” bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 22b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the “Read Command Bypass Mode” bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on IO₀ for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

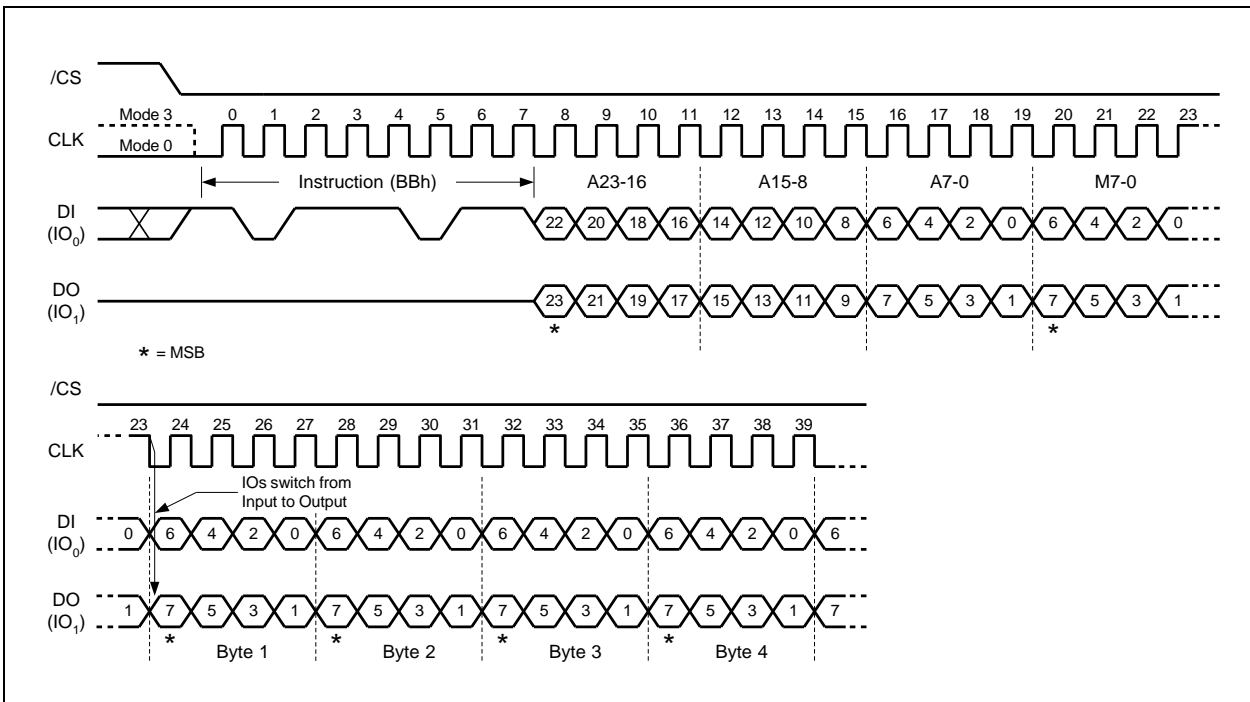


Figure 22a. Fast Read Dual I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

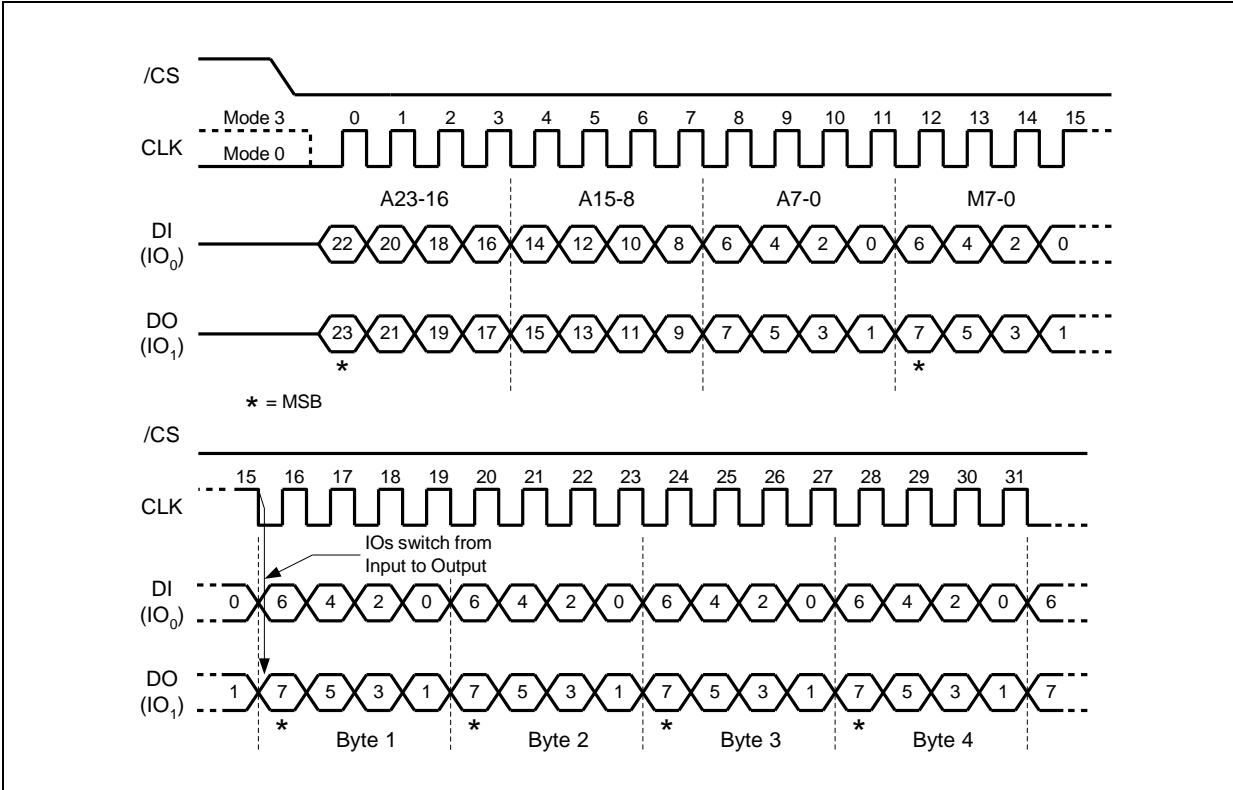


Figure 22b. Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)



8.2.13 DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/O (BDh) instruction allows for improved random access while maintaining two IO pins, IO₀ and IO₁. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

DTR Fast Read Dual I/O with “Read Command Bypass Mode”

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the “Read Command Bypass Mode” bits (M7-0) after the input Address bits (A23-0), as shown in Figure 23a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the “Read Command Bypass Mode” bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 23b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the “Read Command Bypass Mode” bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh/FFFFFFh on IO₀ for the next instruction (16/20 clocks), to ensure M4 = 1 and return the device to normal operation.

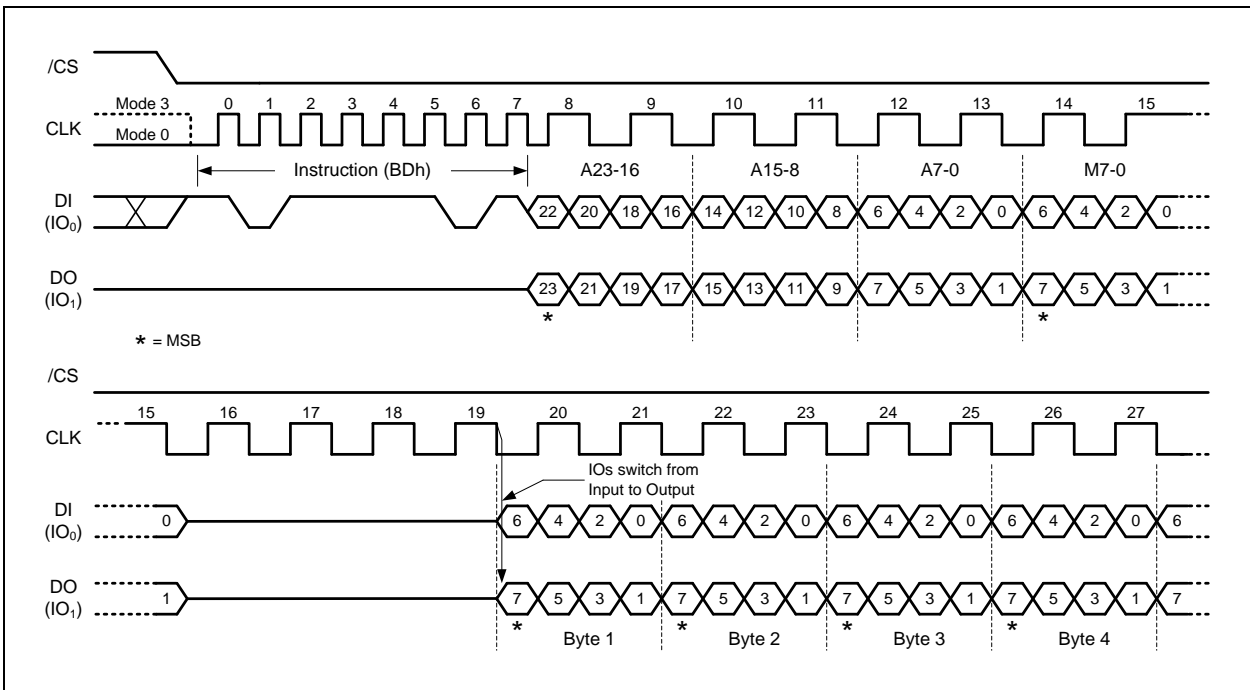


Figure 23a. DTR Fast Read Dual I/O (Initial instruction or previous M5-4≠10, SPI Mode only)

W25Q12PW-DTR

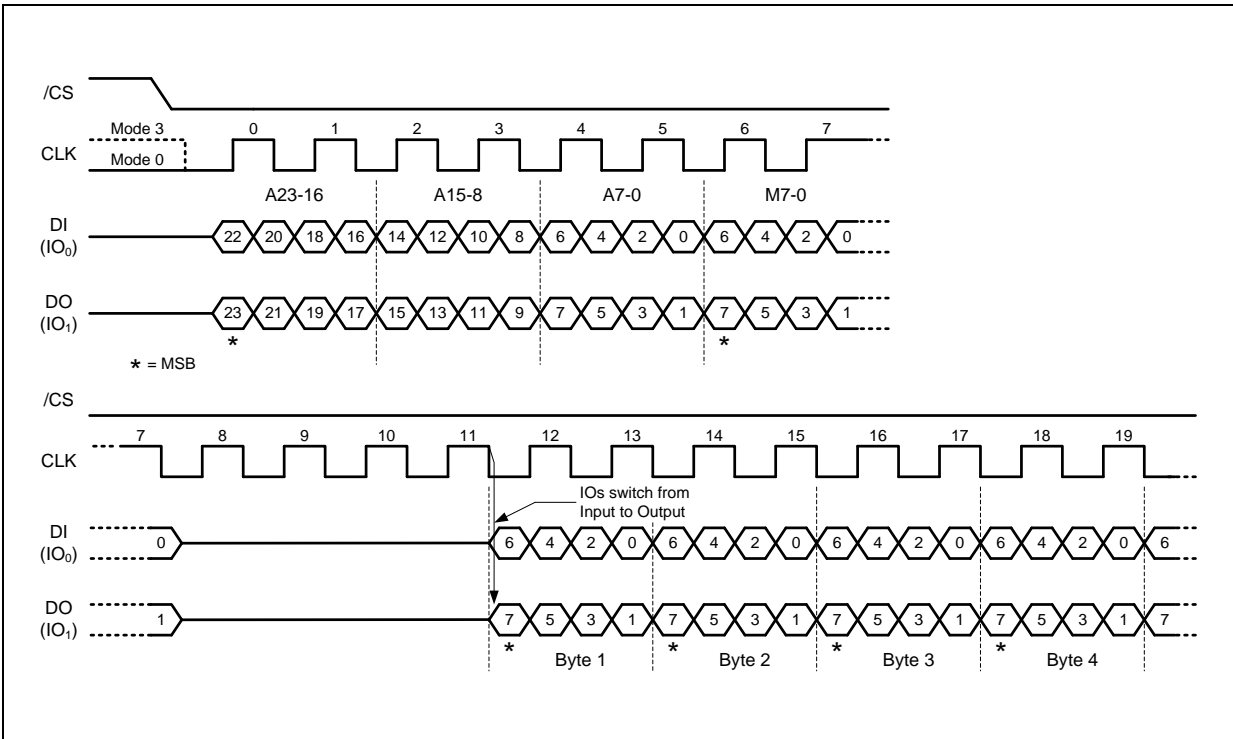


Figure 23b. DTR Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)



8.2.14 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO₀, IO₁, IO₂ and IO₃ and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Fast Read Quad I/O with “Read Command Bypass Mode”

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the “Read Command Bypass Mode” bits (M7-0) after the input Address bits (A23-0), as shown in Figure 24a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the “Read Command Bypass Mode” bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 24b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the “Read Command Bypass Mode” bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

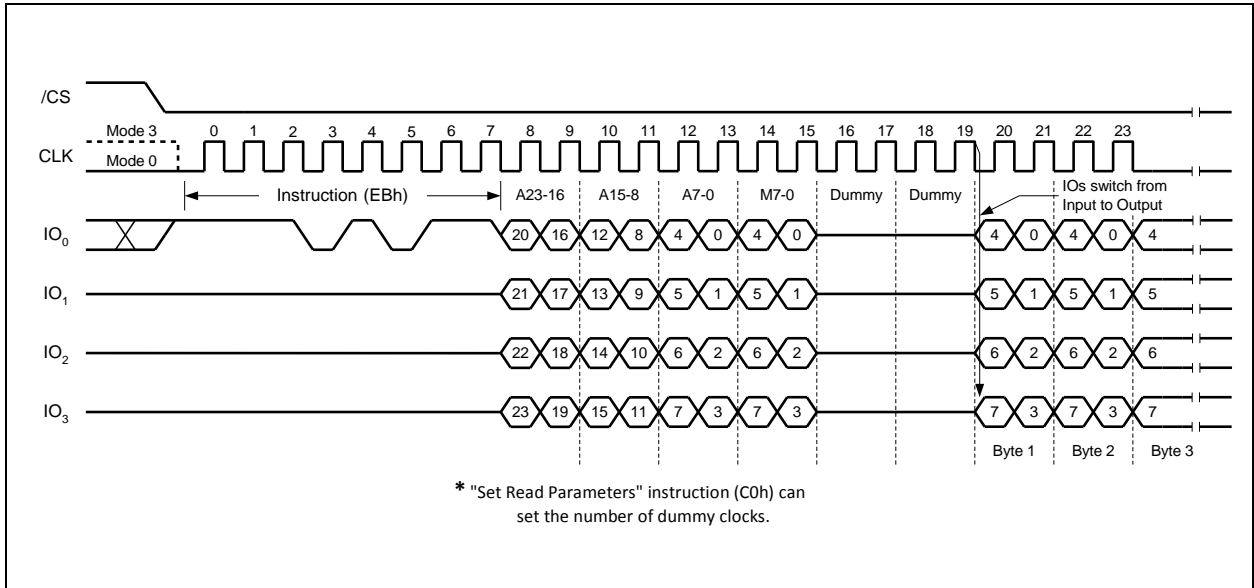


Figure 24a. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10)

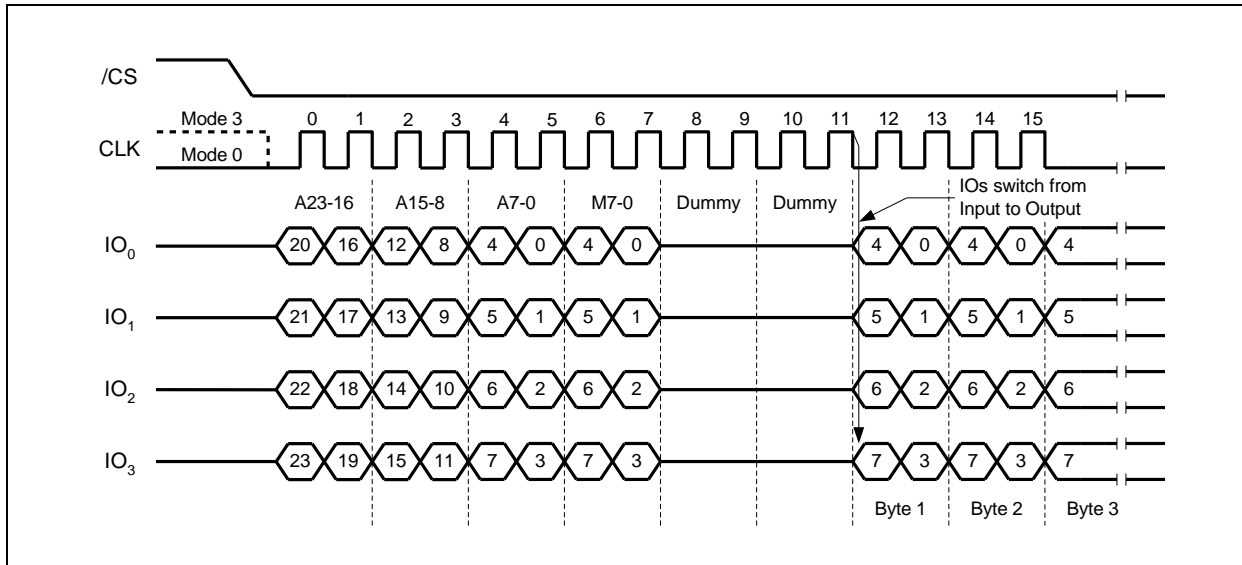


Figure 24b. Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a “Set Burst with Wrap” (77h) command prior to EBh. The “Set Burst with Wrap” (77h) command can either enable or disable the “Wrap Around” feature for the following EBh commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, and once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while bits W6-5 are used to specify the length of the wrap around section within a page. Refer to section 8.2.37 for detail descriptions.



Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 24c. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured as either 6, 8, 10, 12 or 16. The default number of dummy clocks upon power up or after a Reset instruction is 2. In QPI mode, the “Read Command Bypass Mode” bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Read Command Bypass Mode bits immediately.

“Read Command Bypass Mode” feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

“Wrap Around” feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be used. Please refer to “8.2.37 Burst Read with Wrap (0Ch)” for details.

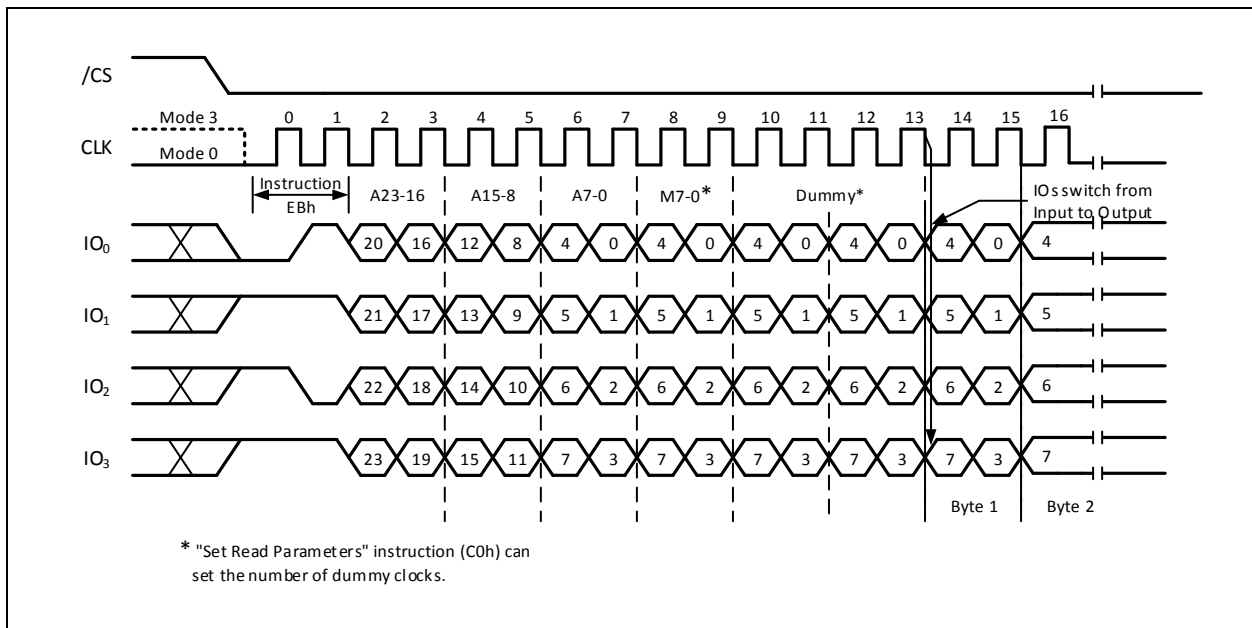


Figure 24c. Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)



8.2.15 DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO₀, IO₁, IO₂ and IO₃ and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

DTR Fast Read Quad I/O with “Read Command Bypass Mode”

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the “Read Command Bypass Mode” bits (M7-0) after the input Address bits (A23/A31-0), as shown in Figure 27a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the “Read Command Bypass Mode” bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 27b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the “Read Command Bypass Mode” bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh/3FFh on IO₀ for the next instruction (8/10 clocks), to ensure M4 = 1 and return the device to normal operation.

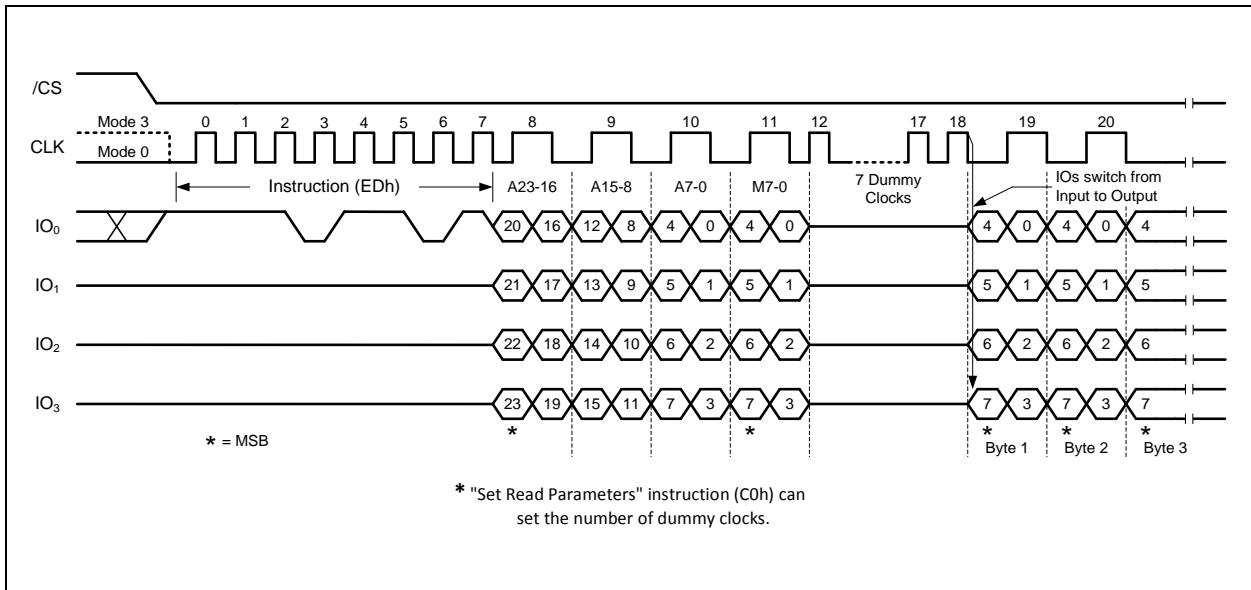


Figure 27a. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, SPI Mode)

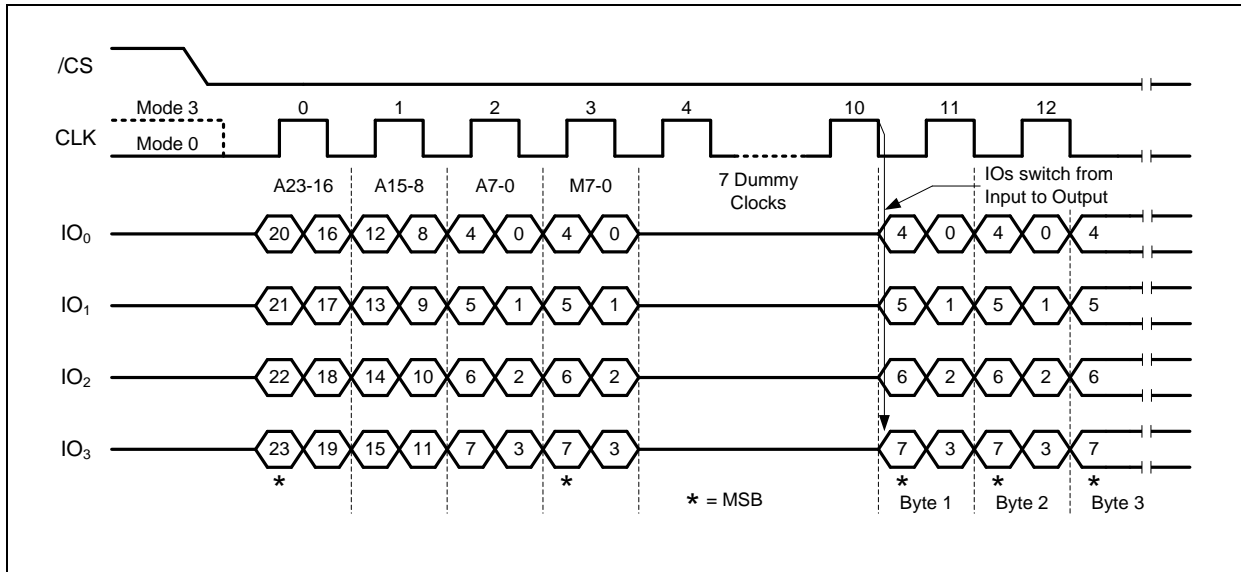


Figure 27b. Fast Read Quad I/O (Previous instruction set M5-4=10, SPI Mode)

DTR Fast Read Quad I/O with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a “Set Burst with Wrap” (77h) command prior to EDh. The “Set Burst with Wrap” (77h) command can either enable or disable the “Wrap Around” feature for the following EDh commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section “8.2.16 Set Burst with Wrap (77h)” for detail descriptions.

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DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 19c. In QPI mode, the “Read Command Bypass Mode” bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Read Command Bypass Mode bits immediately.

“Read Command Bypass Mode” feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

“Wrap Around” feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be used. Please refer to “8.2.37” for details.

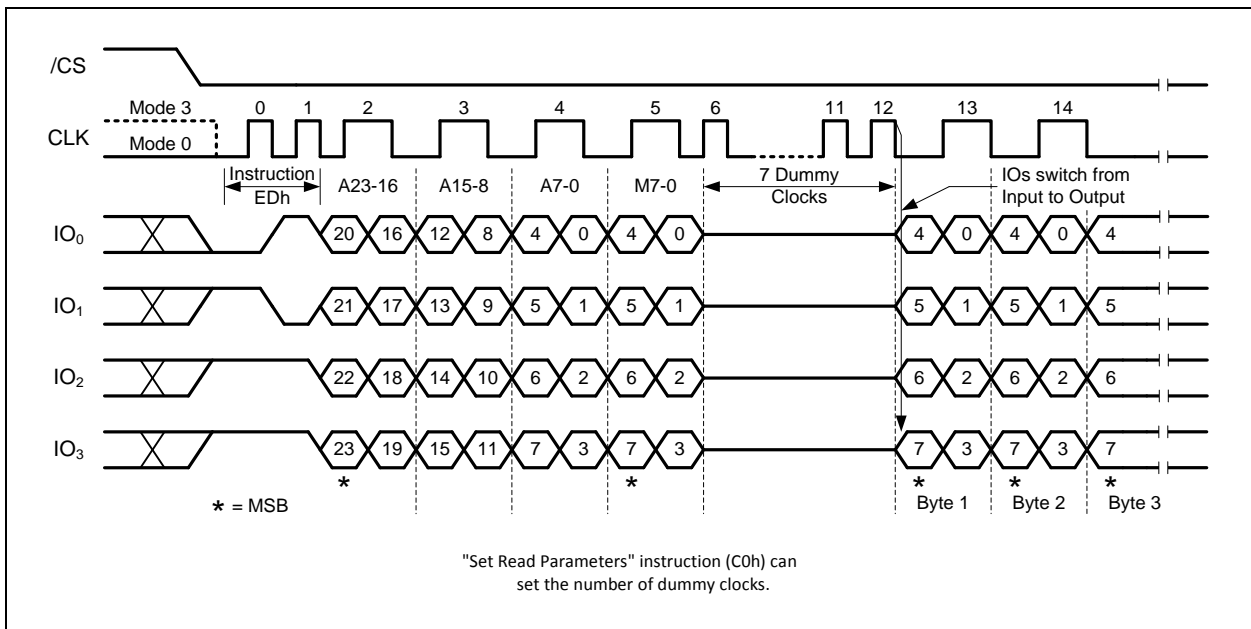


Figure 27c. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)



8.2.16 Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 28. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following “Fast Read Quad I/O” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

In QPI mode, the “Burst Read with Wrap (0Ch)” instruction should be used to perform the Read operation with “Wrap Around” feature. The Wrap Length set by W5-4 in Standard SPI mode is still valid in QPI mode and can also be re-configured by “Set Read Parameters (C0h)” instruction. Refer to the link “8.2.37” and “8.2.37 Burst Read with Wrap (0Ch)” for details.

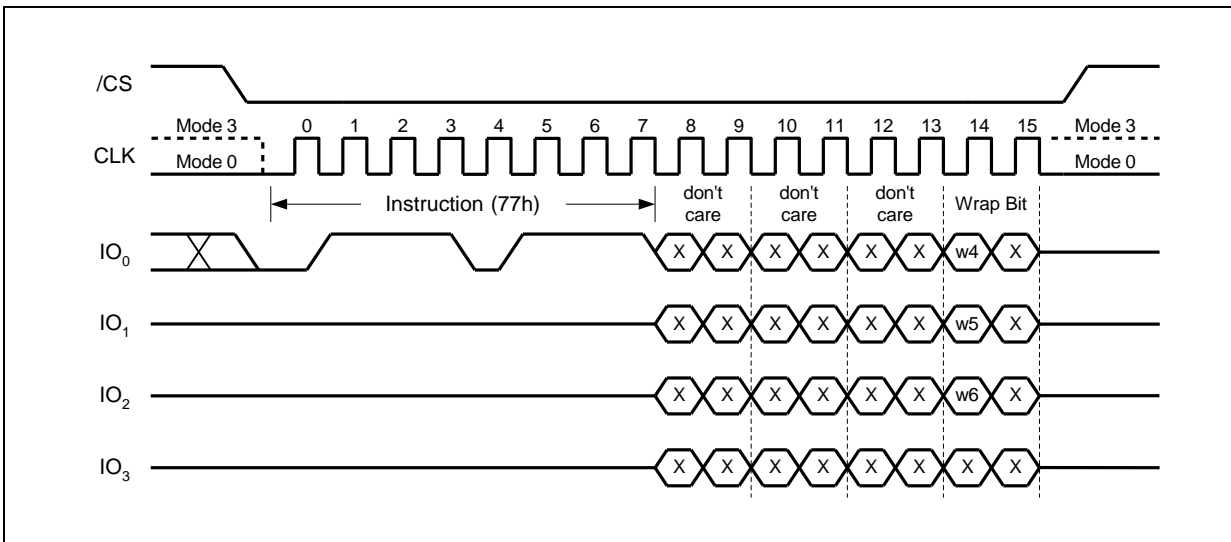


Figure 28. Set Burst with Wrap Instruction (SPI Mode only)



8.2.17 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 29.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of t_{pp} (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Page Program cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

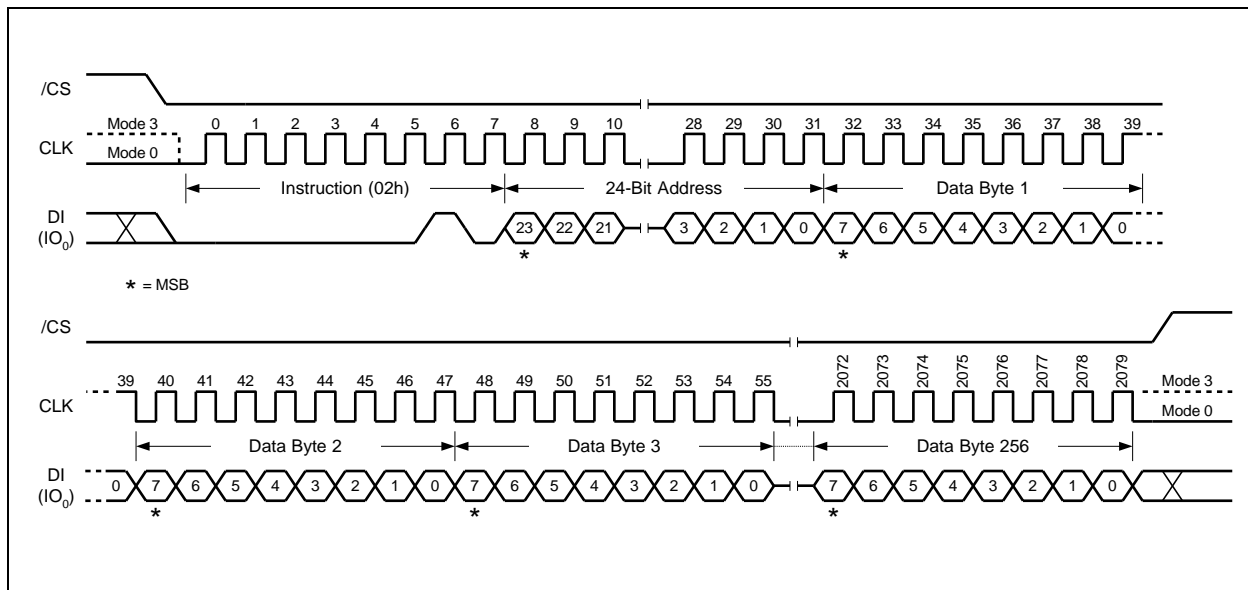


Figure 29a. Page Program Instruction (SPI Mode)



8.2.18 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO₀, IO₁, IO₂, and IO₃. The Quad Page Program can improve performance for PROM Programmers and applications that have slow clock speeds <5MHz. Systems with faster clock speeds will not realize much benefit for from using the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “32h” followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 30.

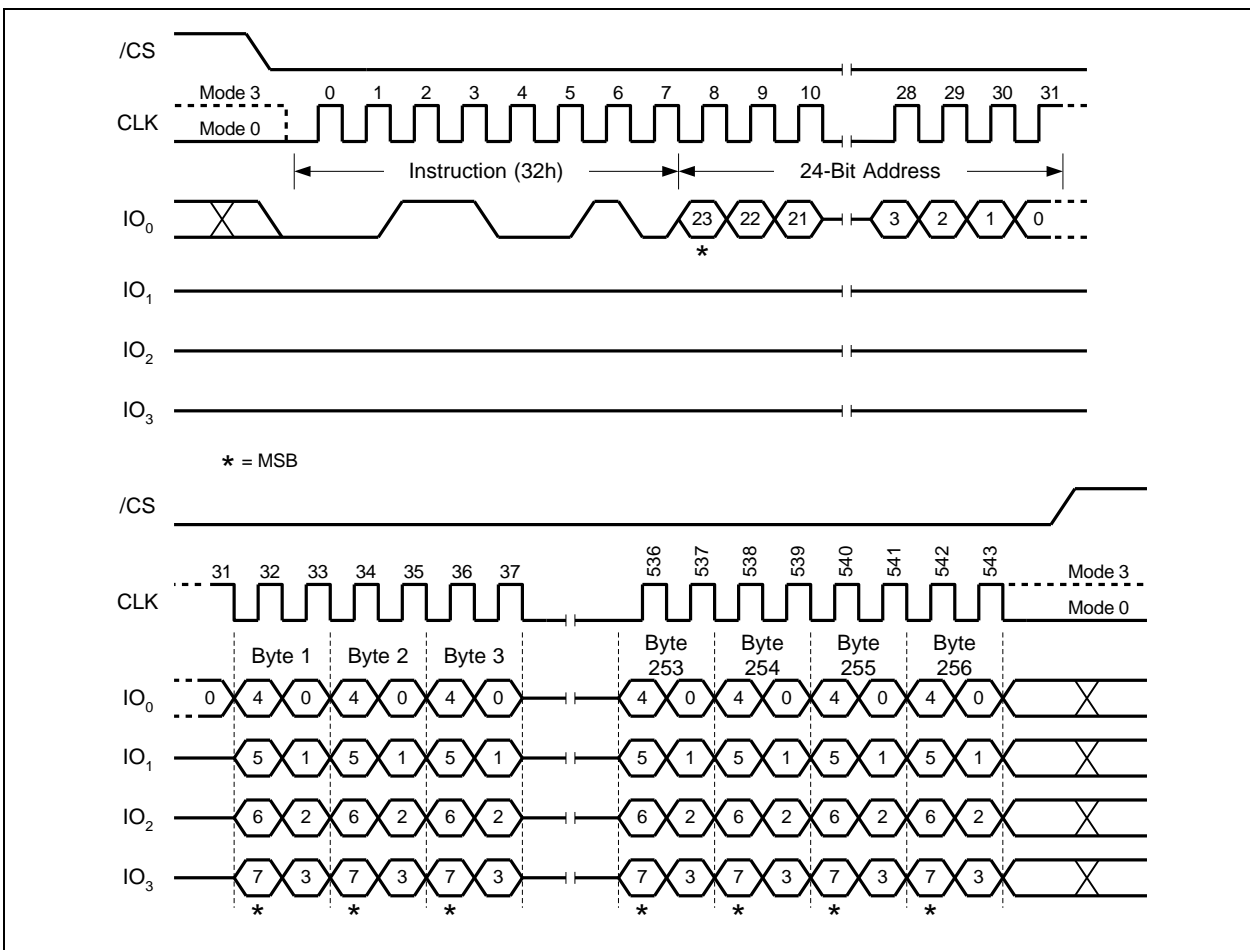


Figure 30. Quad Input Page Program Instruction (SPI Mode only)



8.2.19 Sector Erase (20h)

The Sector Erase instruction sets all bits within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in Figure 31a & 31b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

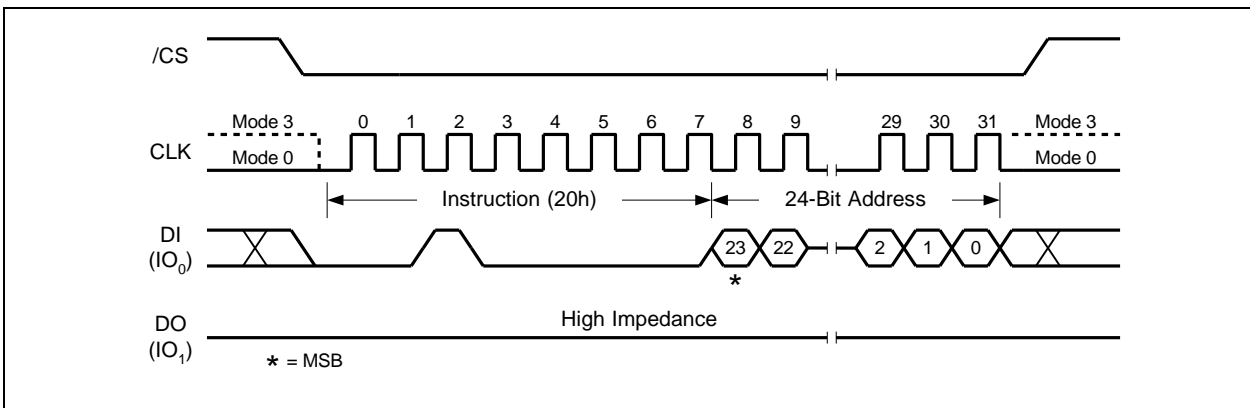


Figure 31a. Sector Erase Instruction (SPI Mode)

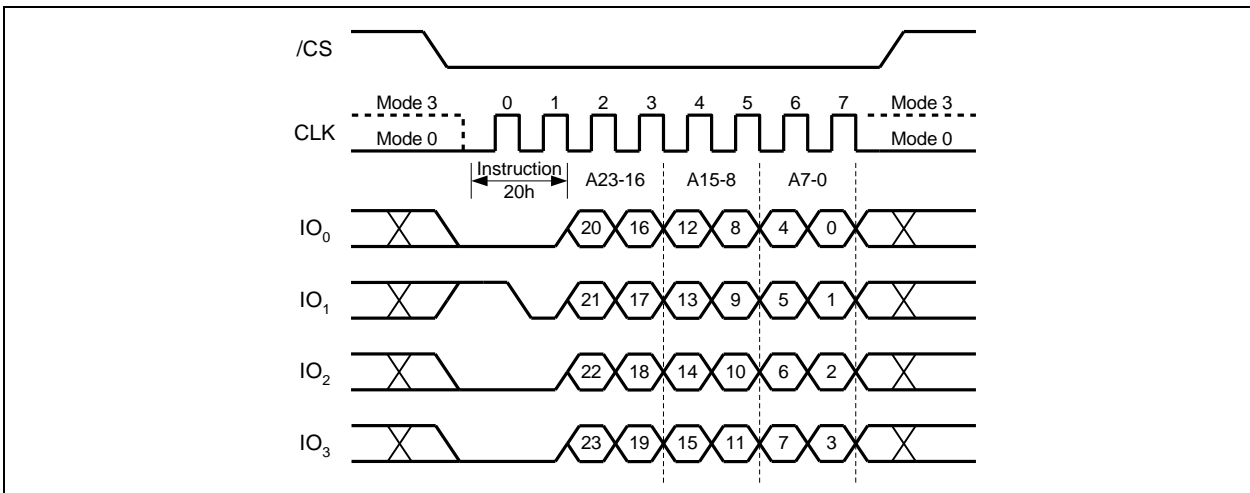


Figure 31b. Sector Erase Instruction (QPI Mode)



8.2.20 32KB Block Erase (52h)

The Block Erase instruction sets all bits within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 32a & 32b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE1 (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

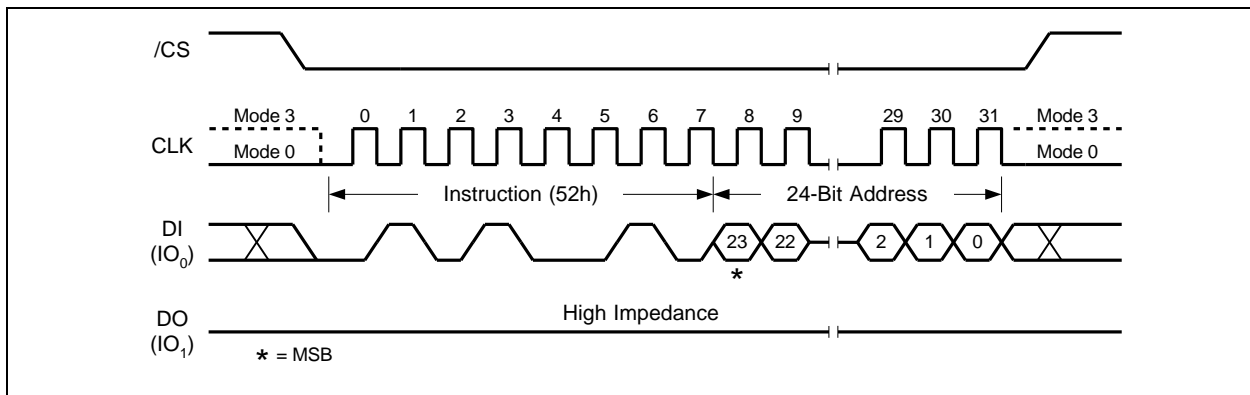


Figure 32a. 32KB Block Erase Instruction (SPI Mode)

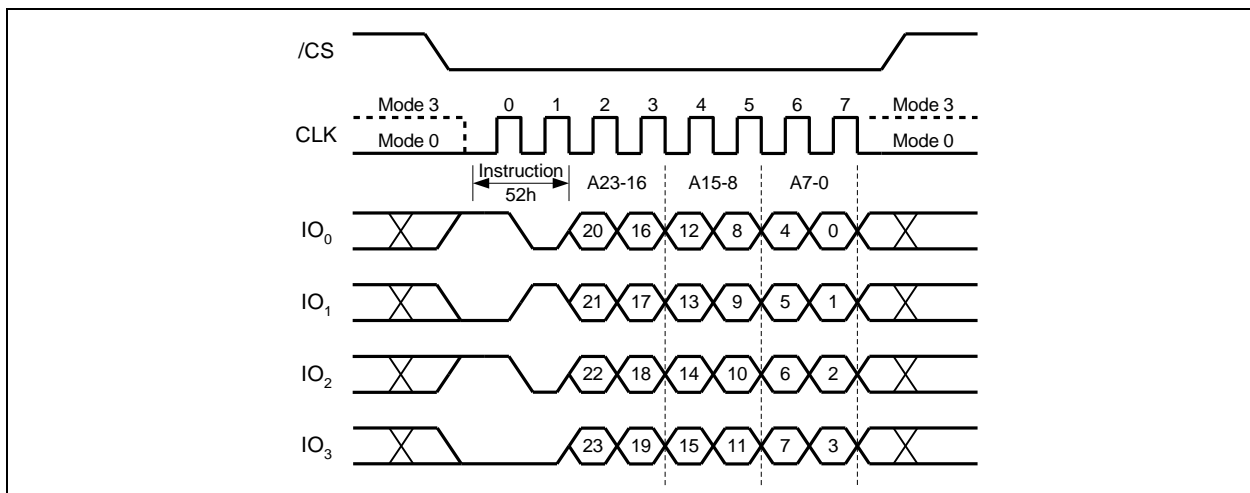


Figure 32b. 32KB Block Erase Instruction (QPI Mode)



8.2.21 64KB Block Erase (D8h)

The Block Erase instruction sets all bits within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 33a & 33b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Block Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

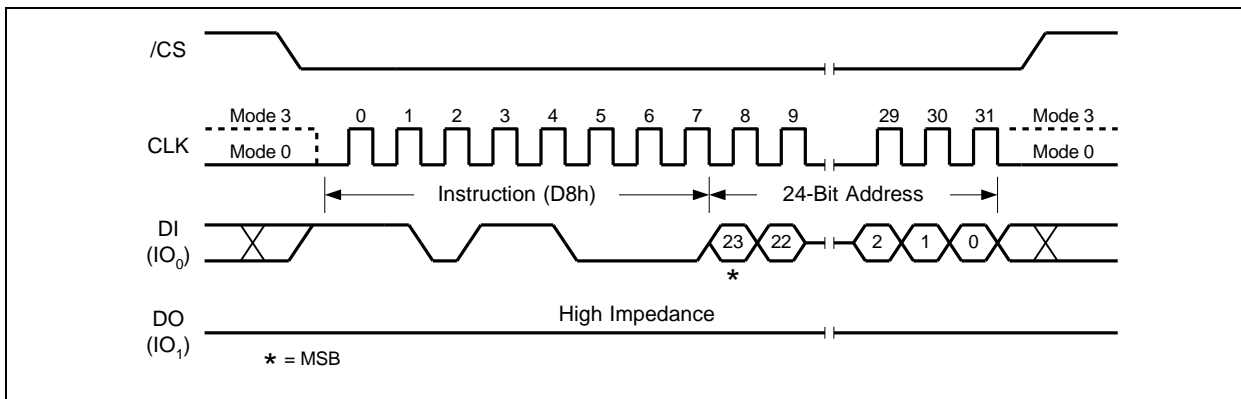


Figure 33a. 64KB Block Erase Instruction (SPI Mode)

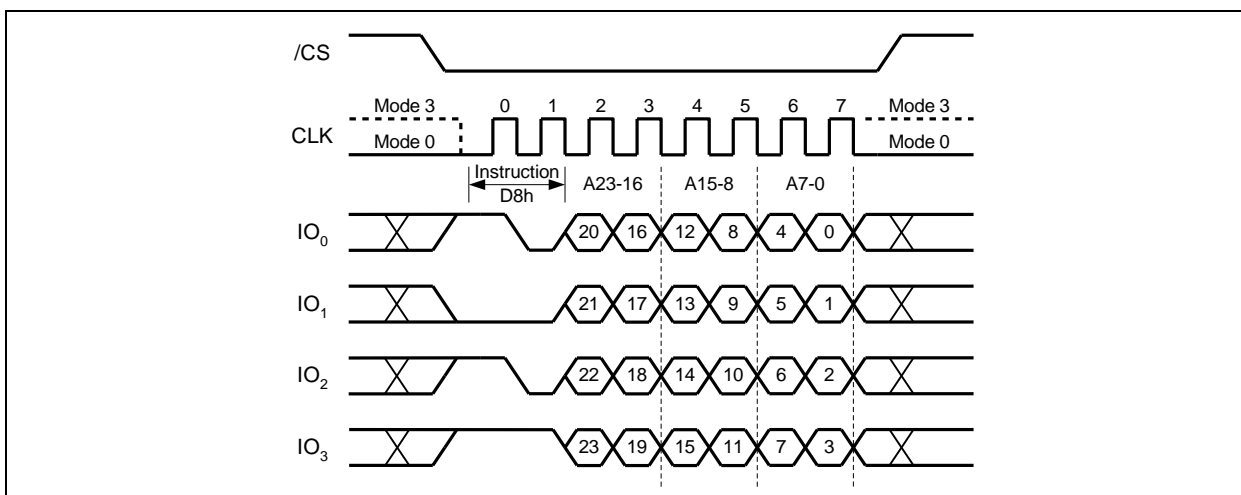


Figure 33b. 64KB Block Erase Instruction (QPI Mode)



8.2.22 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all bits within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 34.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done, the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished, and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

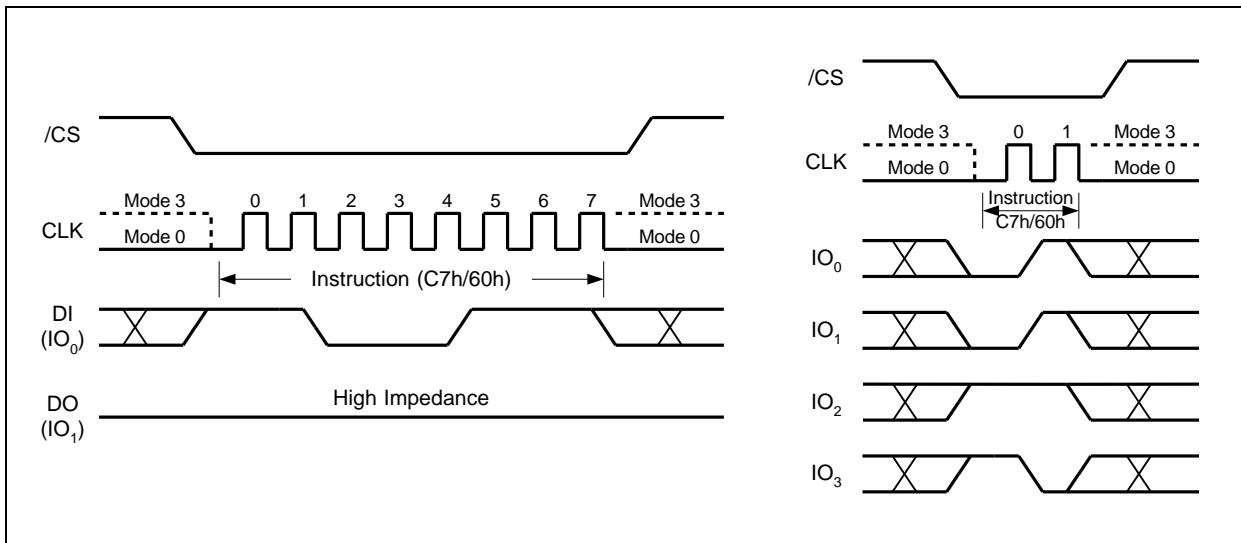


Figure 34. Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)



8.2.23 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 35a & 35b.

The Write Status Register instruction (01h/31h/11h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h/31h/11h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “ t_{SUS} ” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “ t_{SUS} ” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “ t_{SUS} ” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. The SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. The user is recommended to implement design techniques against accidental power interruption and preserve data integrity during the erase/program suspend state.

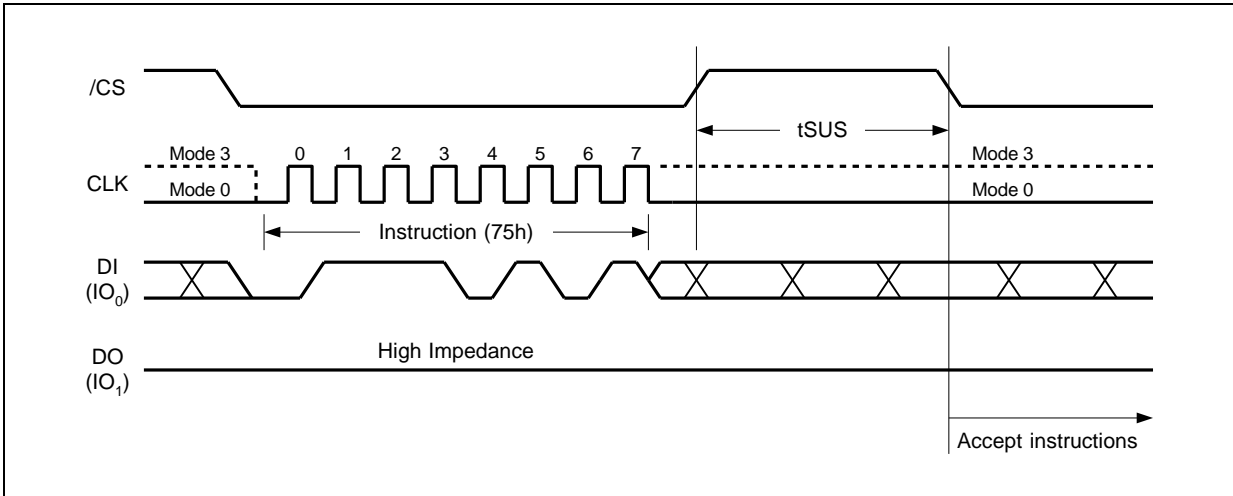


Figure 35a. Erase/Program Suspend Instruction (SPI Mode)

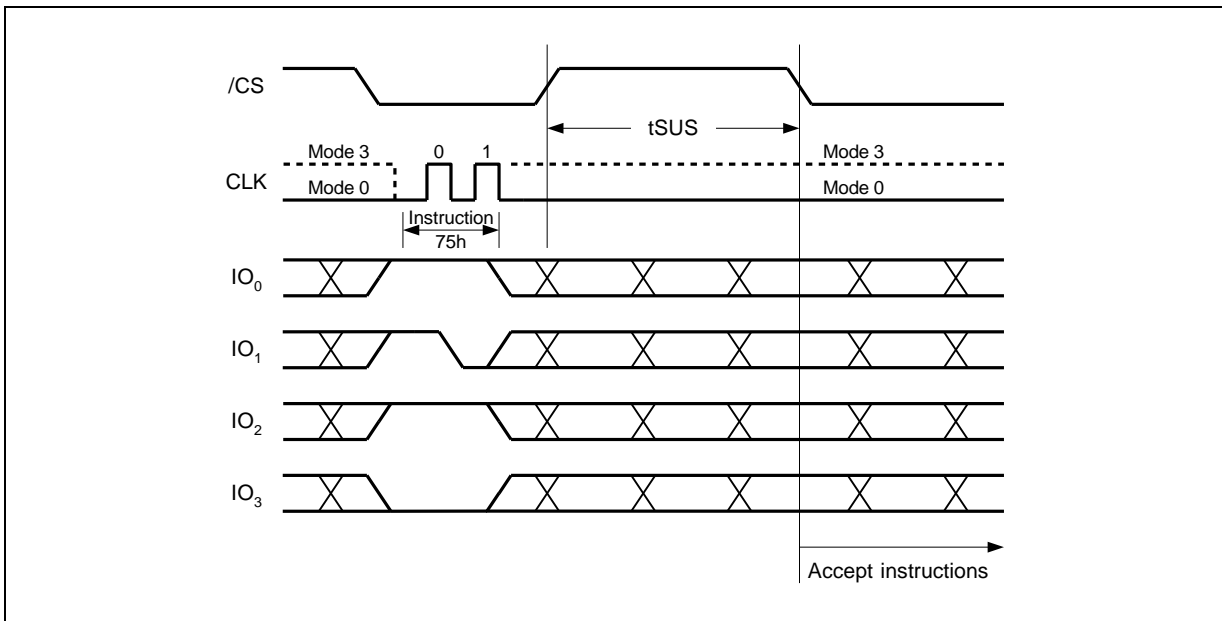


Figure 35b. Erase/Program Suspend Instruction (QPI Mode)



8.2.24 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1, and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 36a & 36b.

The Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by an unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “ t_{sus} ” following a previous Resume instruction.

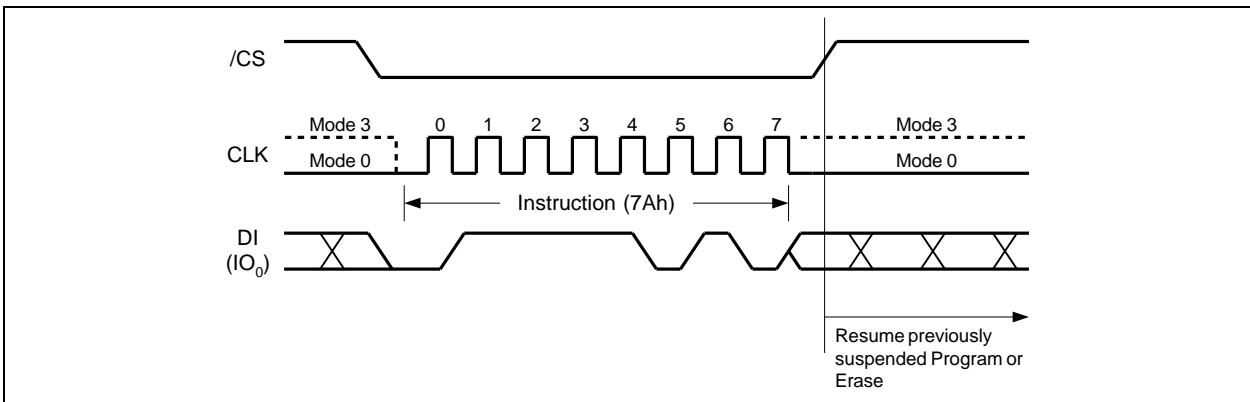


Figure 36a. Erase/Program Resume Instruction (SPI Mode)

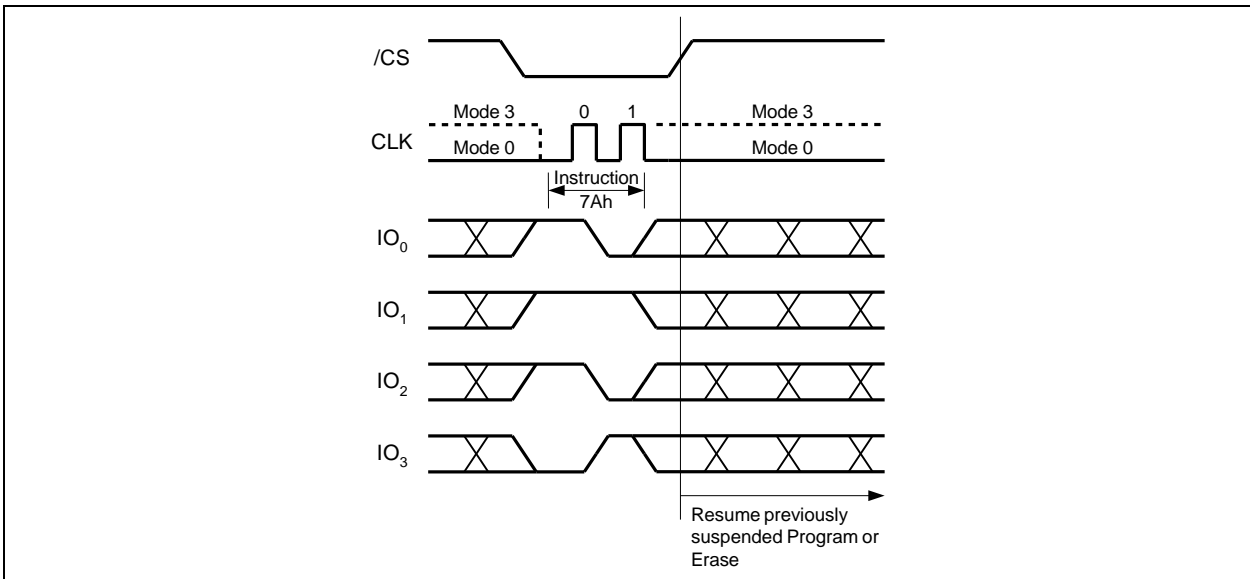


Figure 36b. Erase/Program Resume Instruction (QPI Mode)



8.2.25 Power-down (B9h)

Although the standby current during normal operation is relatively low, the standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 37a & 37b.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done, the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of t_{DP} (See AC Characteristics). While in the power-down state, only the Release Power-down / Device ID (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with a standby current of ICC1.

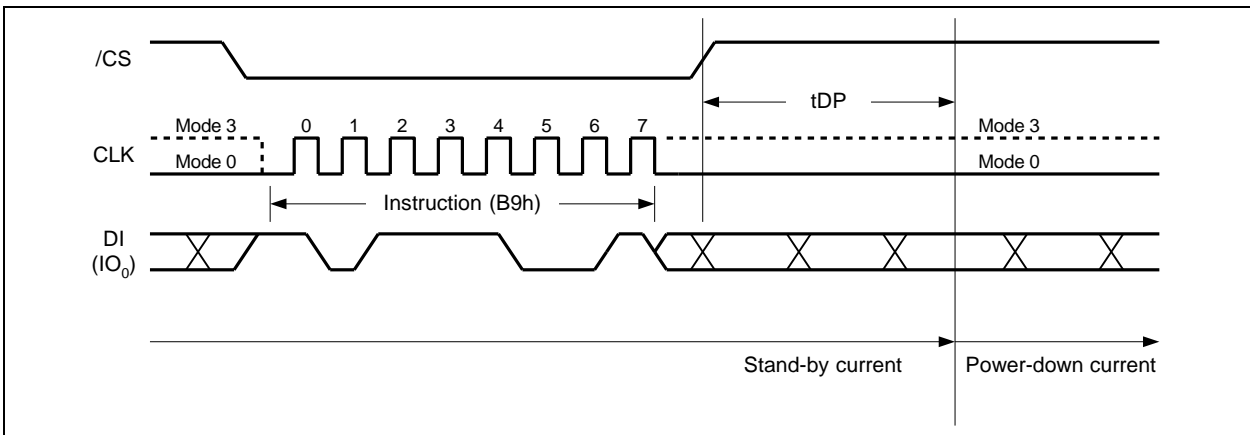


Figure 37a. Deep Power-down Instruction (SPI Mode)

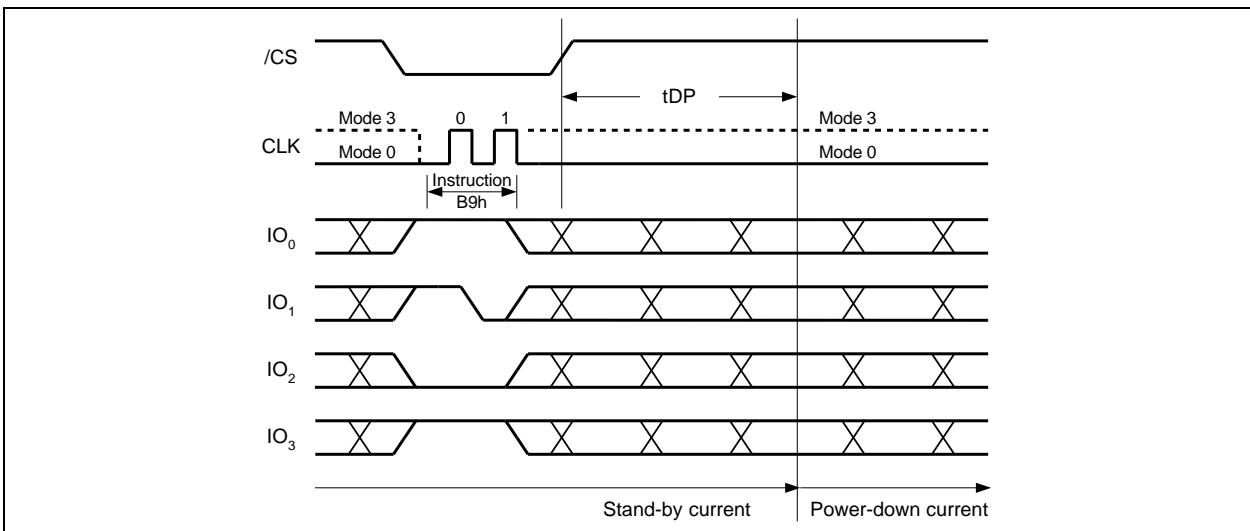


Figure 37b. Deep Power-down Instruction (QPI Mode)



8.2.26 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code "ABh" and driving /CS high as shown in Figure 38a. Release from power-down will take a time of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with the most significant bit (MSB) first. The Device ID value for the W25Q12PW is listed in the Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

If the Release from Power-down instruction is issued while an Erase, Program or Write cycle is in process, (when BUSY equals 1) the instruction is ignored and will not have any effect on the current cycle.

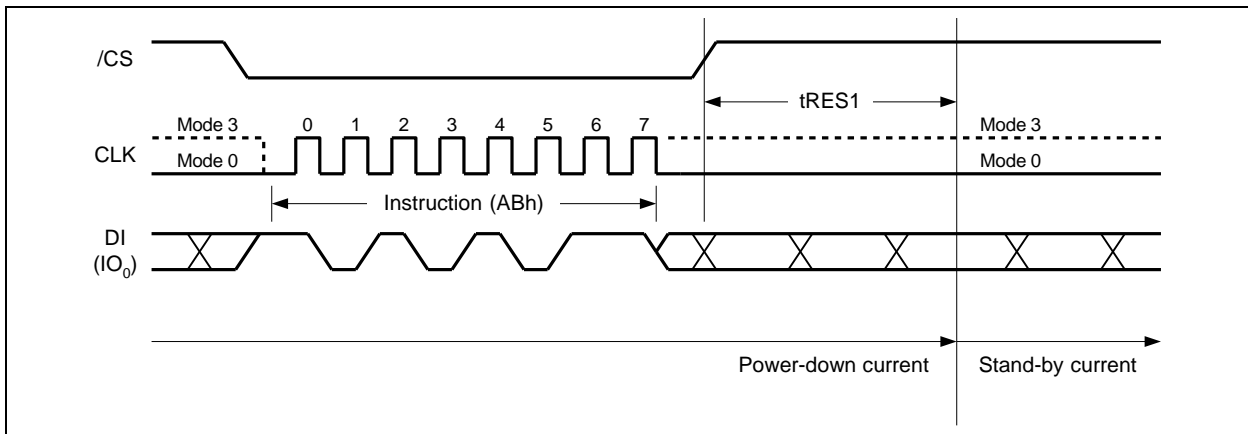


Figure 38a. Release Power-down Instruction (SPI Mode)

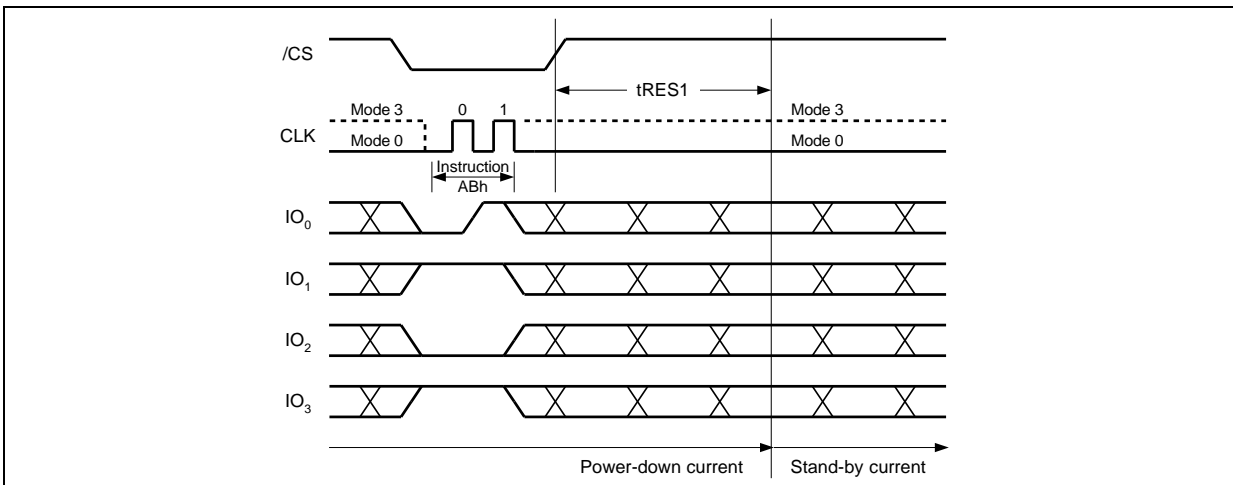


Figure 38b. Release Power-down Instruction (QPI Mode)

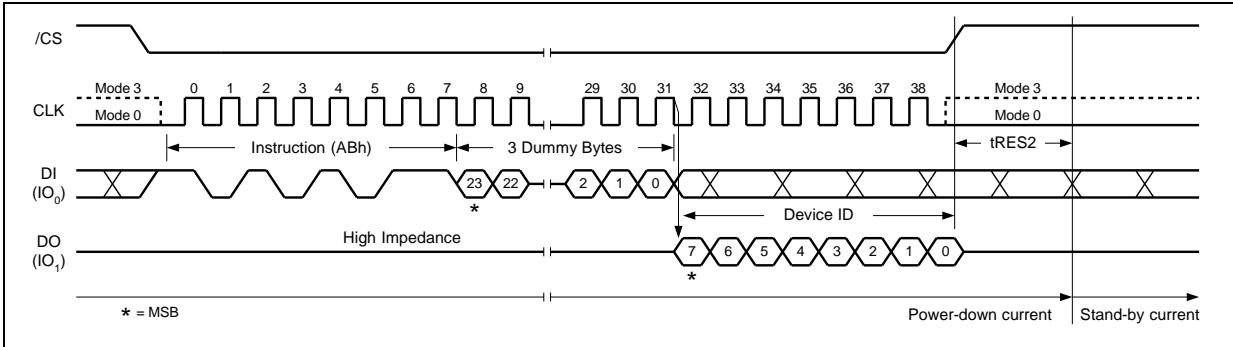


Figure 38c. Device ID Instruction (SPI Mode)

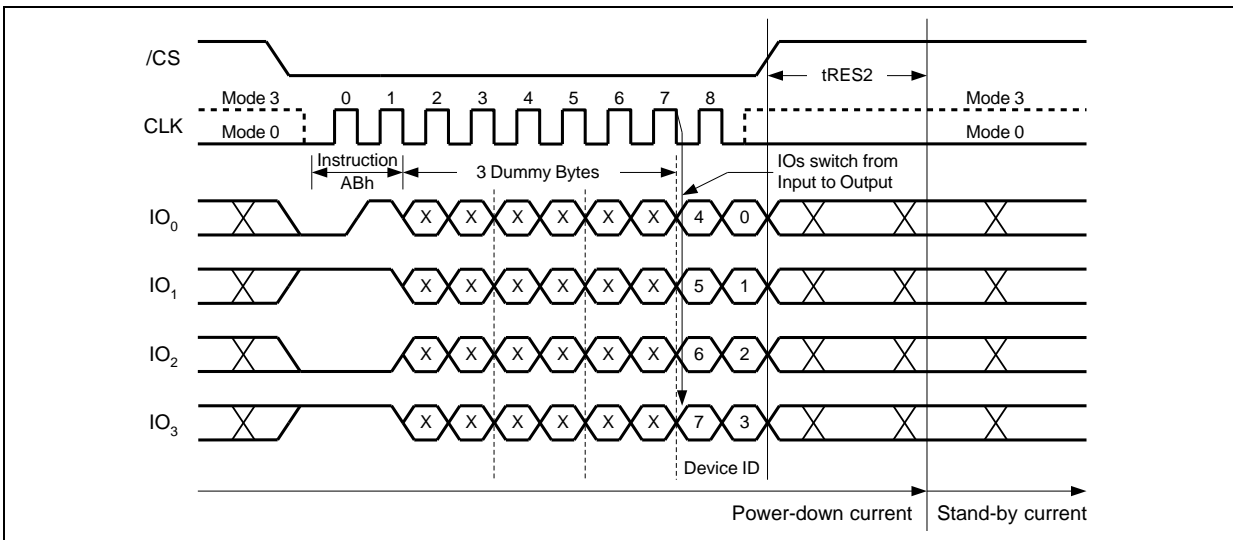


Figure 38d. Device ID Instruction (QPI Mode)

W25Q12PW-DTR



8.2.27 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 39. The Device ID values for the W25Q12PW are listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

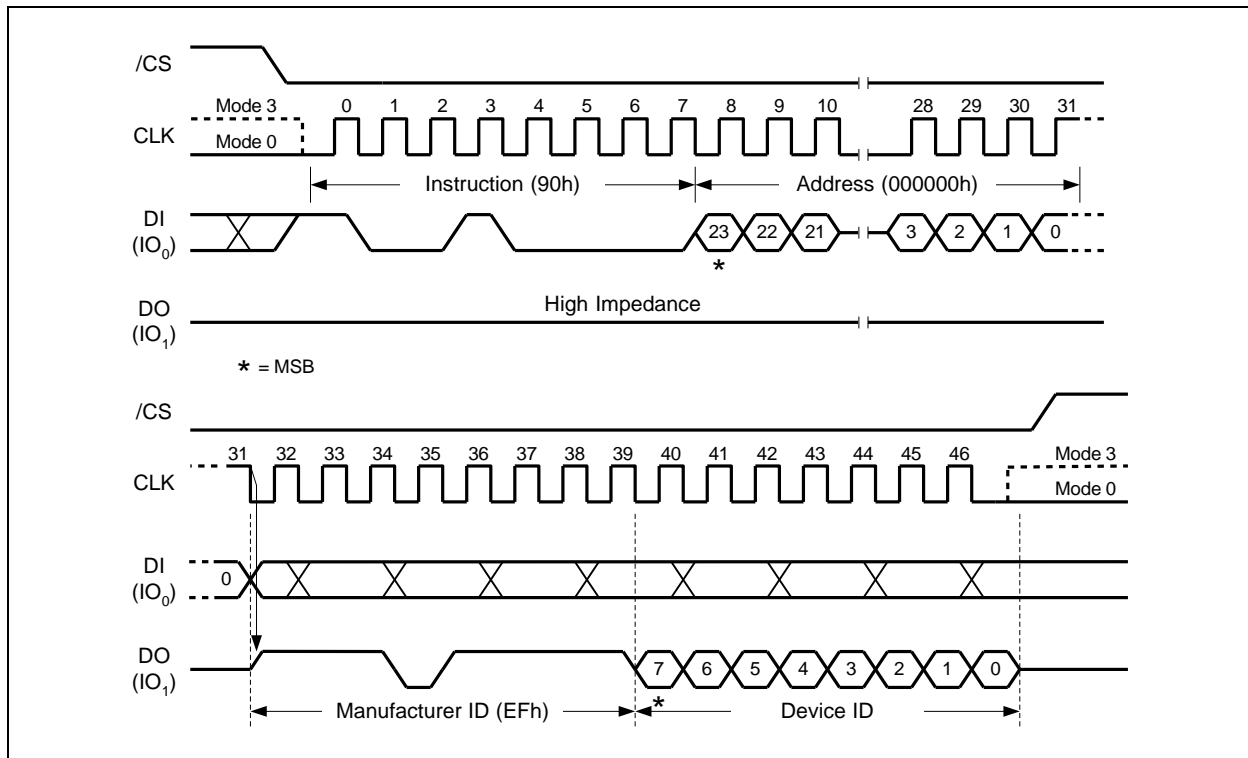


Figure 39. Read Manufacturer / Device ID Instruction (SPI Mode)

W25Q12PW-DTR



8.2.28 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24-bit address (A23-A0) of 000000h, but with the capability to input two bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 40. The Device ID values for the W25Q12PW are listed in the Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

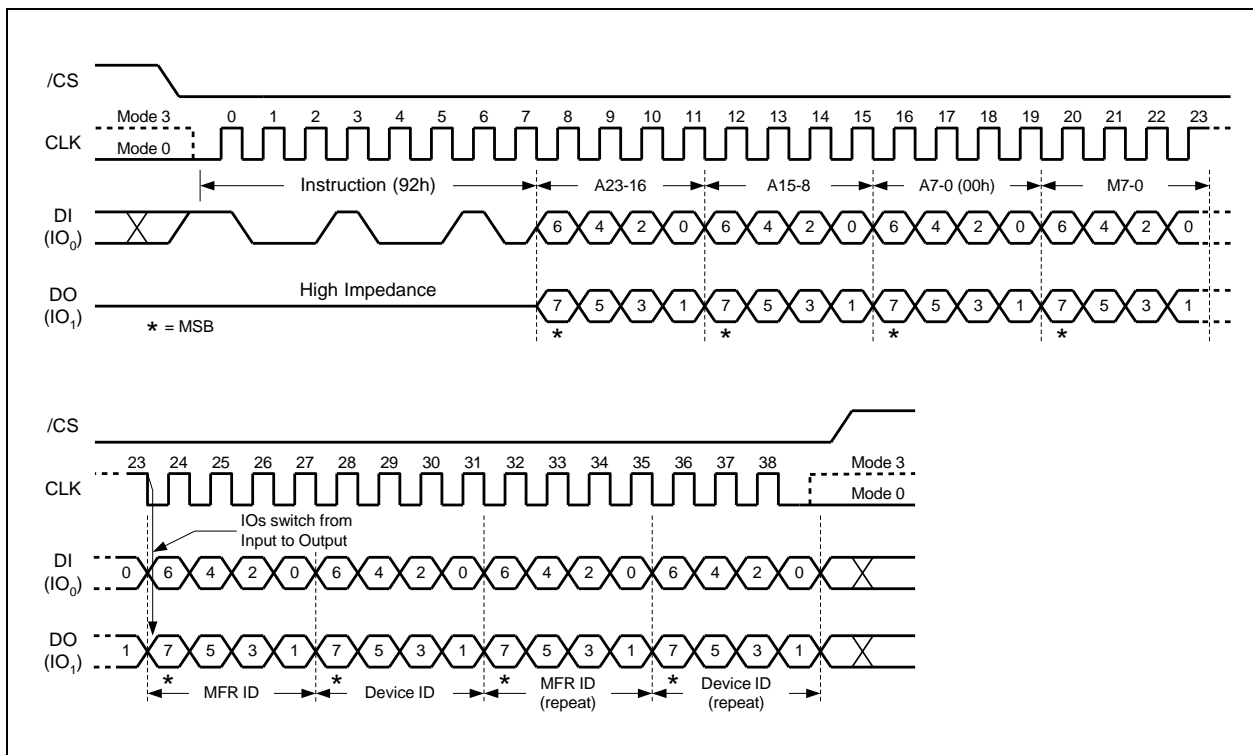


Figure 40. Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)

Note:

The “Read Command Bypass Mode” bits M(7-0) must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

W25Q12PW-DTR



8.2.29 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “94h” followed by a four clock dummy cycles and then a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 41. The Device ID values for the W25Q12PW are listed in the Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

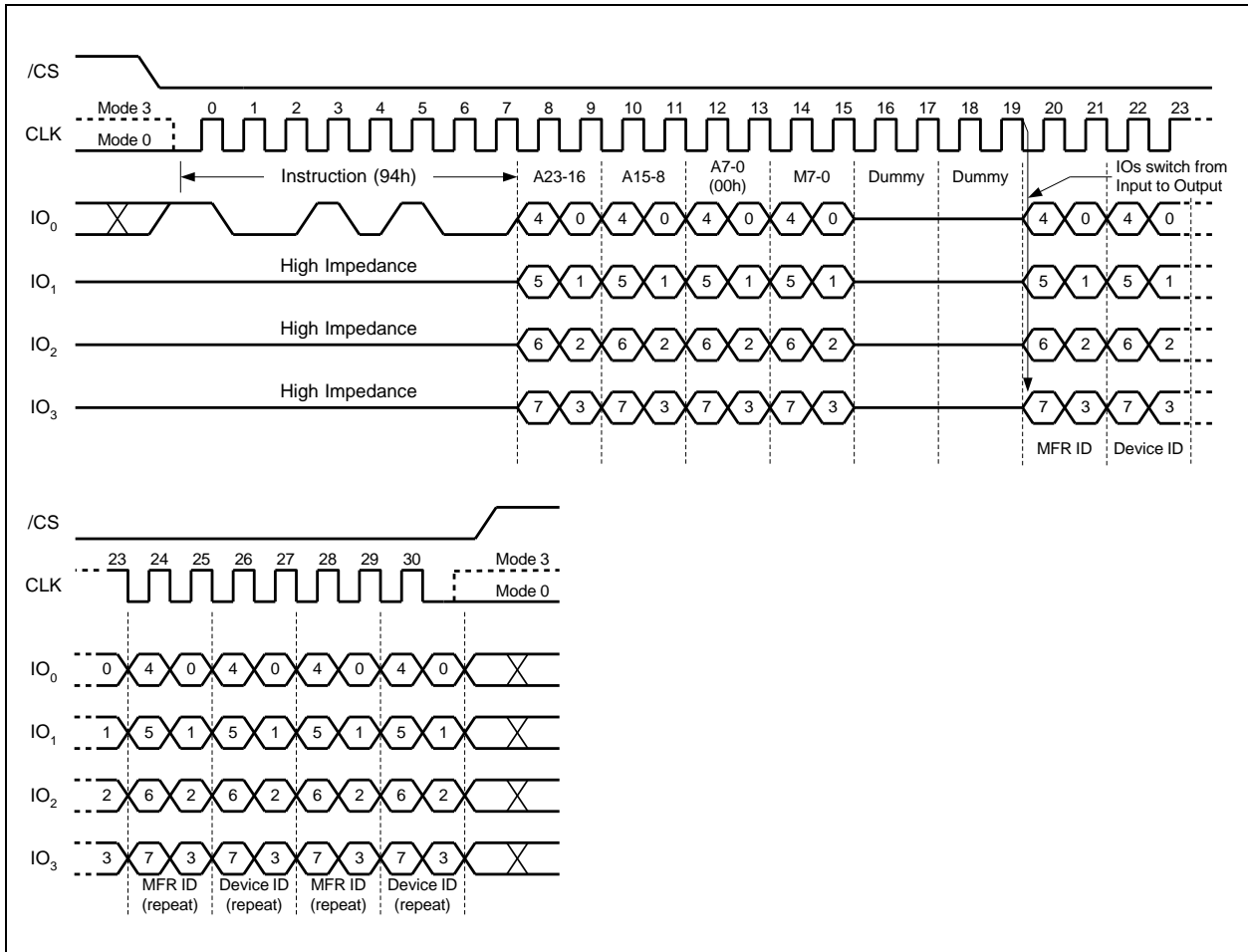


Figure 41. Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)

Note:

The “Read Command Bypass Mode” bits M(7-0) must be set to Fxh to be compatible with Fast Read Quad I/O instruction.



8.2.30 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each W25Q12PW device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 42.

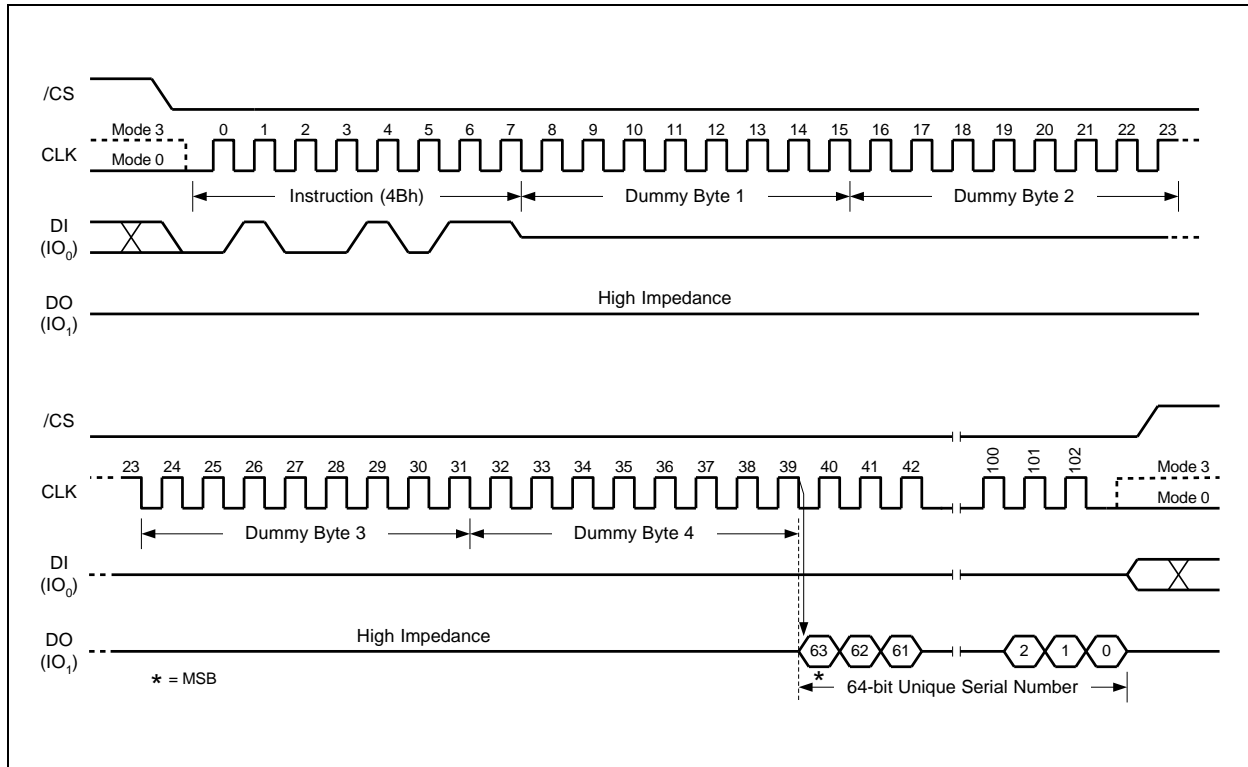


Figure 42. Read Unique ID Number Instruction (SPI Mode only)

W25Q12PW-DTR



8.2.31 Read JEDEC ID (9Fh)

For compatibility reasons, the W25Q12PW provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 43a & 43b. For memory type and capacity values refer to the Manufacturer and Device Identification table.

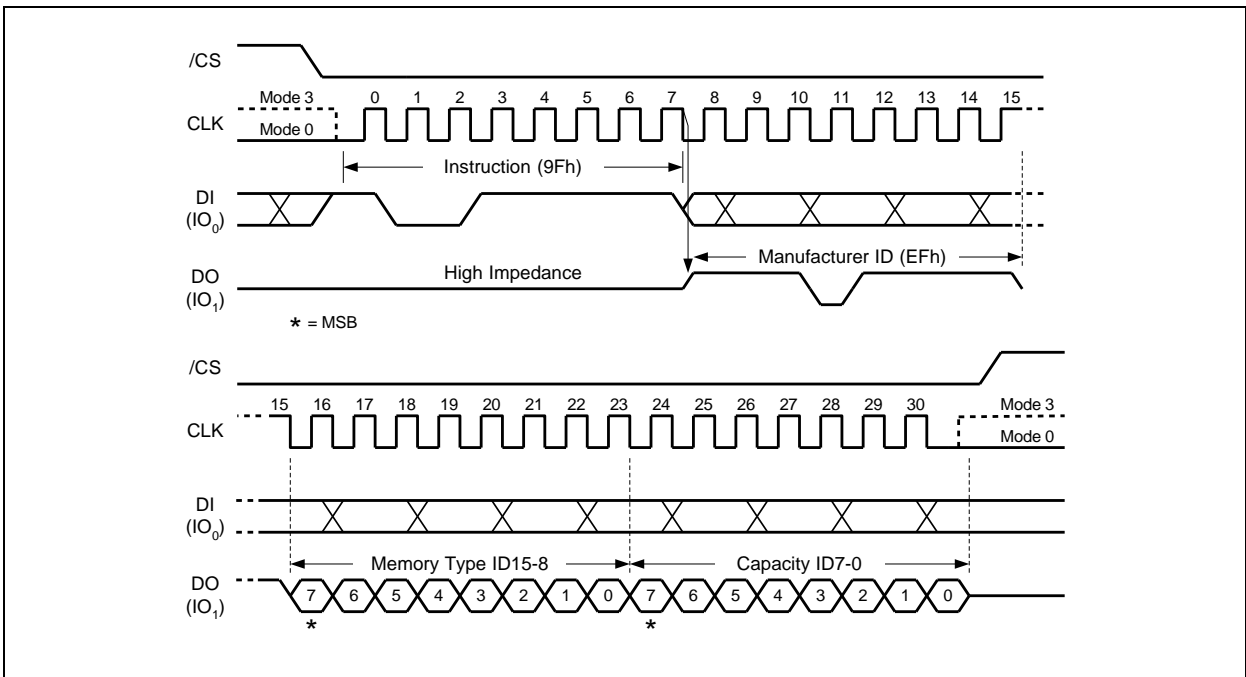


Figure 43a. Read JEDEC ID Instruction (SPI Mode)

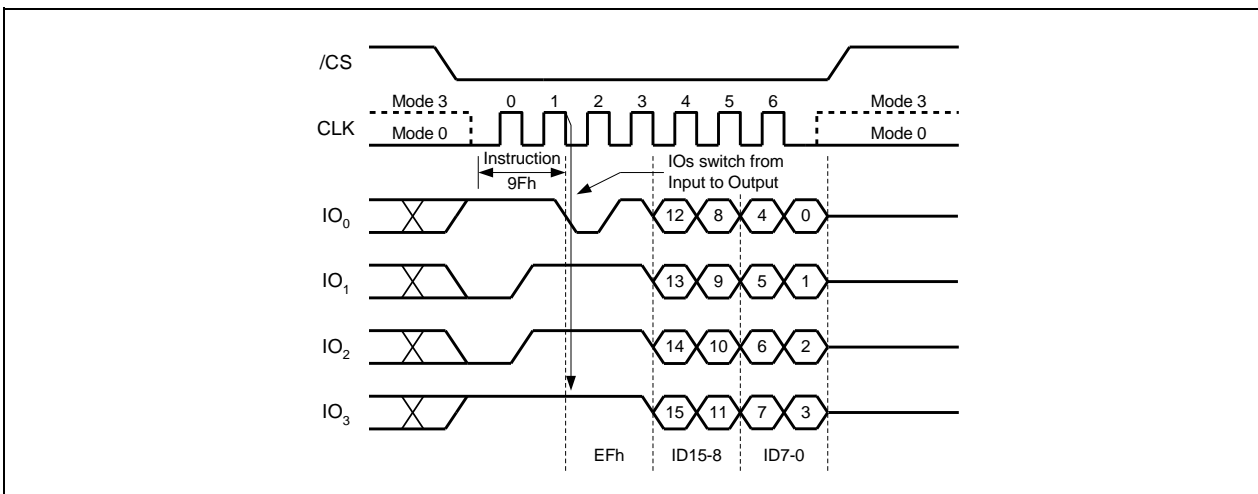


Figure 43b. Read JEDEC ID Instruction (QPI Mode)

W25Q12PW-DTR



8.2.32 Erase Security Registers (44h)

The W25Q12PW offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Don't Care
Security Register #2	00h	0 0 1 0	0 0 0 0	Don't Care
Security Register #3	00h	0 0 1 1	0 0 0 0	Don't Care

The Erase Security Register instruction sequence is shown in Figure 45. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of tSE (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and the Erase Security Register instruction to that register will be ignored (Refer to section 7.1.9 for detail descriptions).

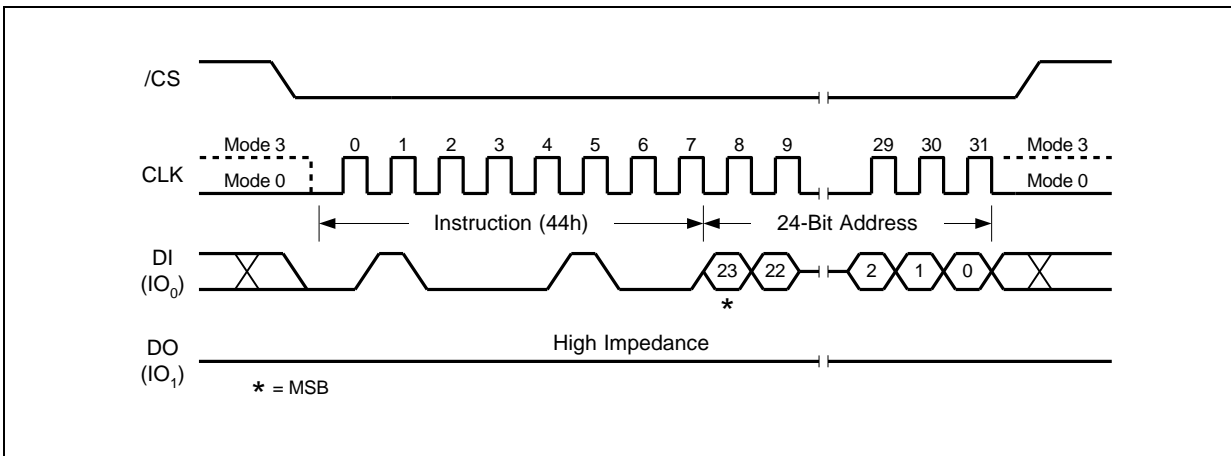


Figure 45. Erase Security Registers Instruction (SPI Mode only)



8.2.33 Read SFDP Register (5Ah)

The W25Q12PW features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216 that is published in 2011. Most Winbond SpiFlash Memories shipped after 2011 (date code 1124 and beyond) support the SFDP feature as specified in the applicable datasheet.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0)⁽¹⁾ into the DI pin. Eight “dummy” clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with the most significant bit (MSB) first as shown in Figure 44. For SFDP register values and descriptions, please refer to the Winbond Application Note for SFDP Definition Table.

Note 1: A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

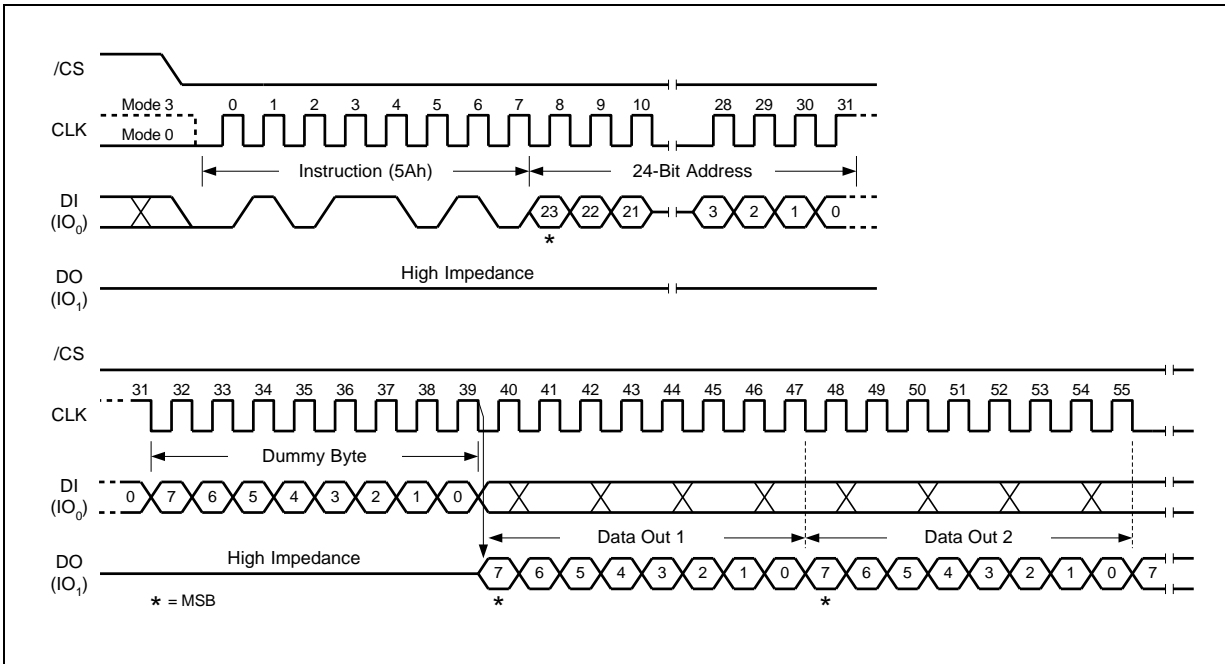


Figure 44a. Read SFDP Register Instruction Sequence Diagram (SPI Mode)

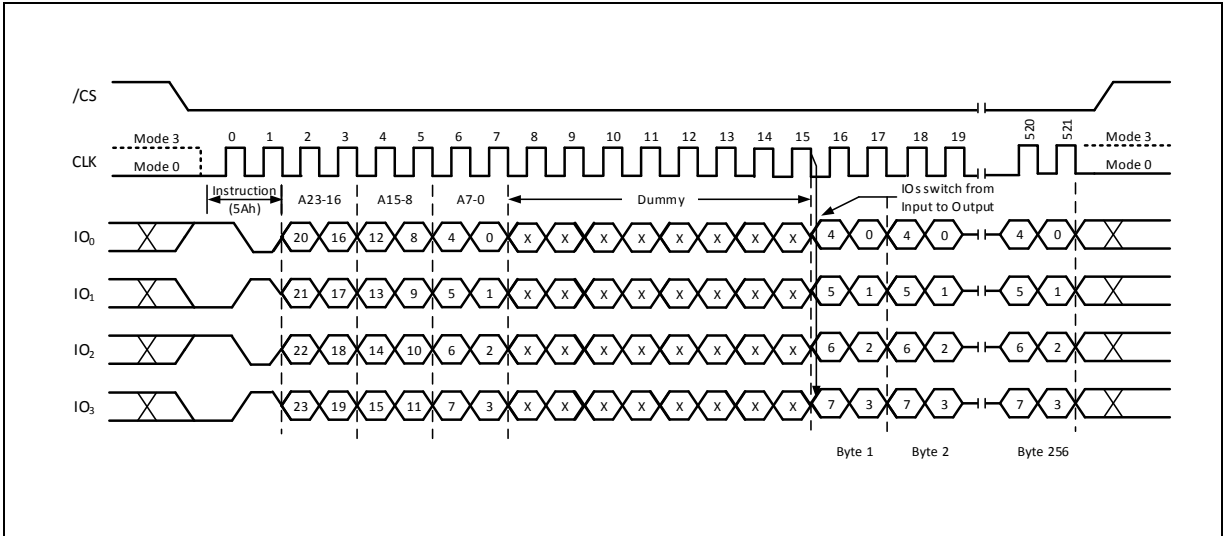


Figure 44b. Read SFDP Register Instruction Sequence Diagram (QPI Mode)



8.2.34 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

The Program Security Register instruction sequence is shown in Figure 46. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and the Program Security Register instruction to that register will be ignored (See “7.1.9 Security Register Lock Bits (LB3, LB2, LB1, LB0) – Non-Volatile OTP Writable” for detail descriptions).

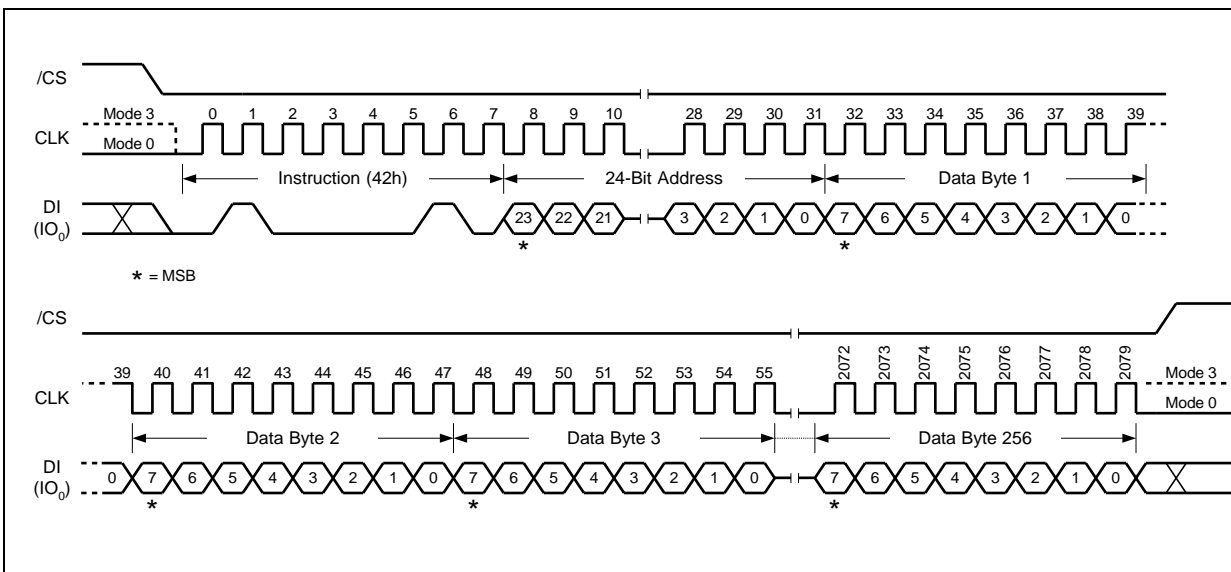


Figure 46. Program Security Registers Instruction (SPI Mode only)



8.2.35 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the four security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 47. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1), the instruction is ignored and will not have any effect on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

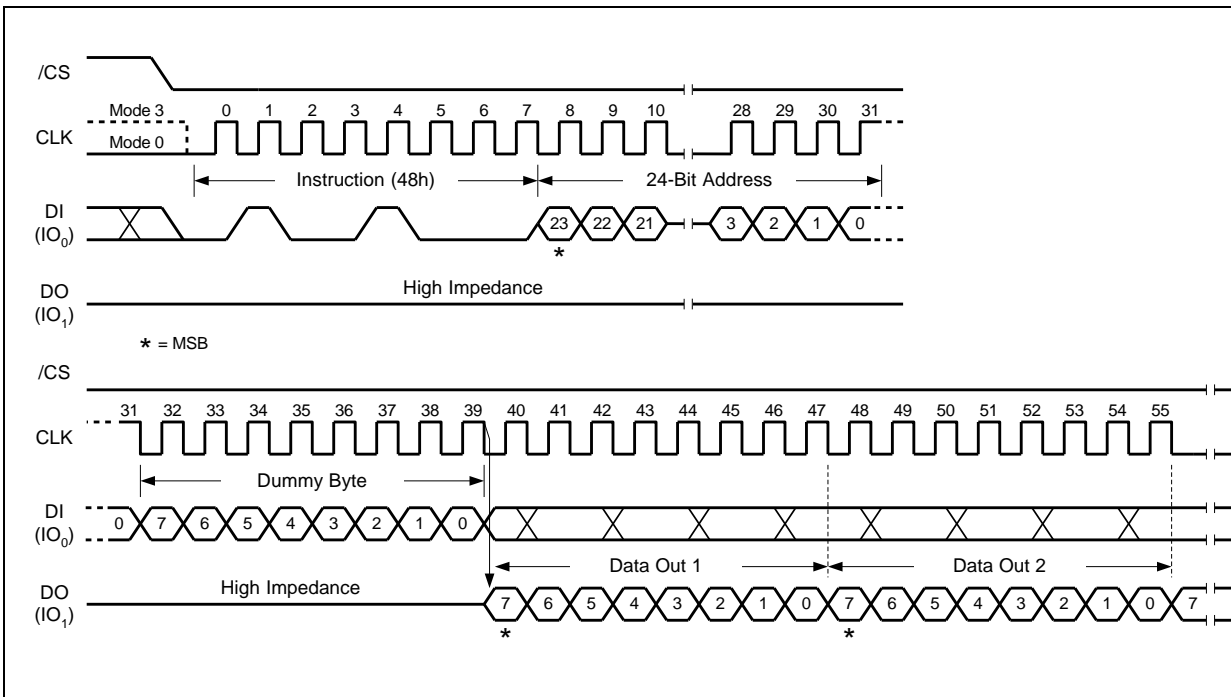


Figure 47. Read Security Registers Instruction (SPI Mode only)



8.2.36 Set Read Parameters (C0h)

“Set Read Parameters (C0h)” instruction is used to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency. This is accomplished by setting the number of dummy clocks and wrap length configurations for set of selected instructions. Set Read Parameters (C0h) instruction writes to the Read Parameter Register (P[7:0]). P[6:4] bits is the dummy clocks configuration, while P[1:0] bits is the wrap length configuration for QPI mode only.

In SPI mode, SPI Set Read Parameters (C0h) instruction writes to ‘Dummy Clocks’ P[6:4] bits only, while it will ignore ‘Wrap Length’ P[1:0] bits as they are don’t care in SPI mode. Conversely, QPI Set Read Parameters instruction will write both to the P[6:4] and P[1:0] Read Parameter bits. The Set Read Parameters instruction sequence is shown in Figure 36.

Set Read Parameters instruction (SPI or QPI) is used to configure the number of dummy cycles through P[6:4] Read Parameter bits for the following SPI, QPI, DTR, and QPI DTR instructions:

- Standard SPI mode: Fast Read Quad I/O (EBh) instruction
- QPI mode: Fast Read (0Bh), Fast Read Quad I/O (EBh), and Burst Read with Wrap (0Ch) instructions
- SPI DTR mode: DTR Fast Read Quad I/O (EDh)
- QPI DTR mode: DTR Fast Read (0Dh) in QPI mode, DTR Fast Read Quad I/O (EDh) in QPI mode, and DTR Burst Read with Wrap (0Eh) in QPI mode instructions.

In QPI mode only, Set Read Parameters instruction to P[1:0] Read Parameter bits is used to configure the “Wrap Length” for the following QPI and QPI DTR read with wrap instructions:

- QPI mode: Burst Read with Wrap (0Ch) instruction
- QPI DTR mode: DTR Burst Read with Wrap (0Eh) instruction.

QPI “Wrap Length” (P[1:0] bits) is the field setting for the number of bytes to burst read (8, 16, 32, or 64 bytes) before a wrap-around to the starting address. . The Wrap Length set by P[1:0] is only applicable in QPI mode and not in SPI mode. The “Fast Read Quad I/O (EBh)”, “Fast Read (0Bh)”, “DTR Fast Read Quad I/O (EDh)”, and “DTR Fast Read (0Dh)” instructions do not support wrap around feature in QPI mode.

The dummy clocks for various Fast Read instructions in Standard/Dual/Quad/DTR SPI mode are fixed, except for “Fast Read Quad I/O (EBh)”, and “DTR Fast Read Quad I/O (EDh)” instructions. Please refer to the Instruction Tables 1-4 and 7-8 for details. “Wrap Length” for the SPI “Fast Read Quad I/O (EBh)” and “DTR Fast Read Quad I/O (EDh)” instructions is set by the W6-4 bits with the “Set Burst with Wrap (77h)” instruction.

The Wrap bits (Set Burst with Wrap ‘77h’) as well as Read Parameter bits P[7:0] setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode or vice versa. It is very important that the required dummy cycles and wrap length are set properly before executing the SPI (EBh), QPI (0Bh, EBh, 0Ch), DTR (EDh), and QPI DTR (0Dh, EDh, 0Eh) instructions.

The default Parameter Read “Dummy Clocks” and “Wrap Length” settings for selected SPI, QPI, DTR, and QPI DTR read instructions after power up or reset are defined in the tables below. After power up or reset, Read Parameter bits are reset to 00h. Detailed Read Parameter bits configuration are also shown below.

QPI/QPI DTR Wrap Length:

QPI: 0Ch /QPI DTR: 0Eh

P1 – P0	WRAP LENGTH (QPI: 0Ch QPI DTR: 0Eh)
0 0	8-byte ⁽¹⁾
0 1	16-byte
1 0	32-byte
1 1	64-byte

Dummy Clocks and Wrap Length Configurations

W25Q12PW-DTR



SPI/QPI Dummy Clocks:

P6 – P4	Dummy Clocks (SPI: EBh)	MAX. READ FREQ. ⁽²⁾
0 0 0	6	133MHz ⁽¹⁾
0 0 1	6	133MHz
0 1 0	6	133MHz
0 1 1	8	133MHz
1 0 0	10	133MHz
1 0 1	12	166MHz
1 1 0	14	166MHz
1 1 1	16	166MHz

P6 – P4	Dummy Clocks (QPI: 0Bh/EBh/0Ch)	MAX. READ FREQ. ⁽²⁾
0 0 0	6	133MHz ⁽¹⁾
0 0 1	6	133MHz
0 1 0	6	133MHz
0 1 1	8	133MHz
1 0 0	10	133MHz
1 0 1	12	166MHz
1 1 0	14	166MHz
1 1 1	16	166MHz

DTR/QPI DTR Dummy Clocks:

P6 – P4	Dummy Clocks (SPI DTR: EDh)	MAX. READ FREQ. ⁽²⁾
0 0 0	8	104MHz ⁽¹⁾
0 0 1	8	104MHz
0 1 0	8	104MHz
0 1 1	8	104MHz
1 0 0	10	104MHz
1 0 1	12	104MHz
1 1 0	14	104MHz
1 1 1	16	104MHz

P6 – P4	Dummy Clocks (QPI DTR: 0Dh/EDh/0Eh)	MAX. READ FREQ. ⁽²⁾
0 0 0	8	104MHz ⁽¹⁾
0 0 1	8	104MHz
0 1 0	8	104MHz
0 1 1	8	104MHz
1 0 0	10	104MHz
1 0 1	12	104MHz
1 1 0	14	104MHz
1 1 1	16	104MHz

Notes:

1. Default from power up
2. Required address alignment and start address for Reads: LSB A[1:0]=00b

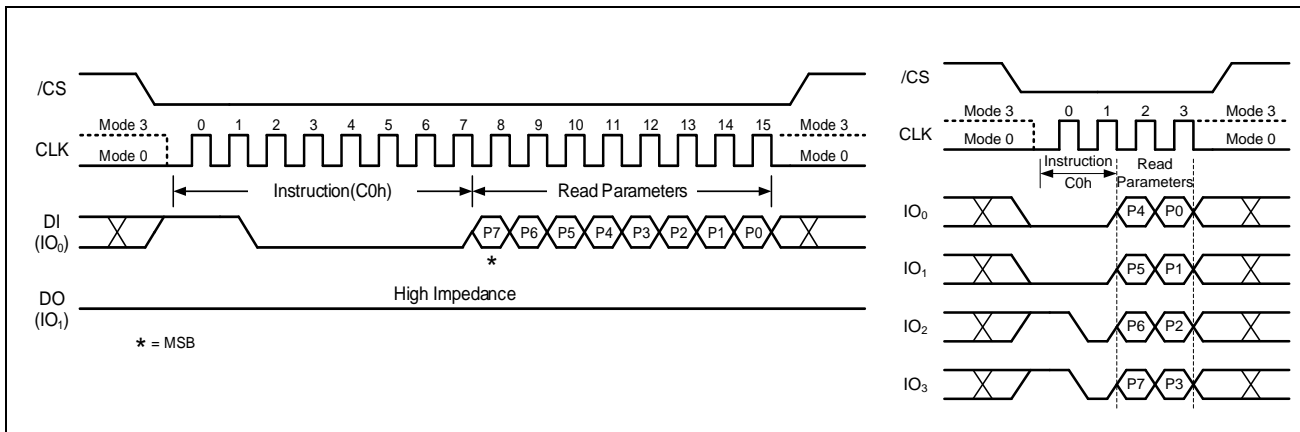


Figure48. Set Read Parameters (C0h) Instruction for SPI Mode (left) or QPI Mode (right)

* SPI Set Read Parameters(C0h) instruction writes to "Dummy Clock" P[6:4] bit only. It will ignore Warp Length P[0:1] bits input was they are don't care in SPI mode.



8.2.38 DTR Burst Read with Wrap (0Eh)

The “DTR Burst Read with Wrap (0Eh)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “DTR Fast Read (0Dh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “DTR Burst Read with Wrap” instruction also has configurable number of “Dummy Clocks” and “Wrap Length”; and they are configured by the “Set Read Parameters (C0h)” instruction. The Read Parameter bits have to be set with the desired number of dummy cycles and wrap length prior to the DTR Burst Read with Wrap operation.

The Read Parameter Bits P[6:4] setting determines the number of dummy clocks and can be either 8, 10, 12, 14, or 16. The default number of dummy clocks upon power up or after a Reset instruction is 8. The Read Parameter Bits P[1:0] setting determines the “Wrap Length” (8, 16, 32, or 64 bytes). The output data starts at the initial address specified in the instruction, and once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command. The Burst Read with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. Refer to Section 8.2.36 for detail descriptions on “Set Read Parameters”.

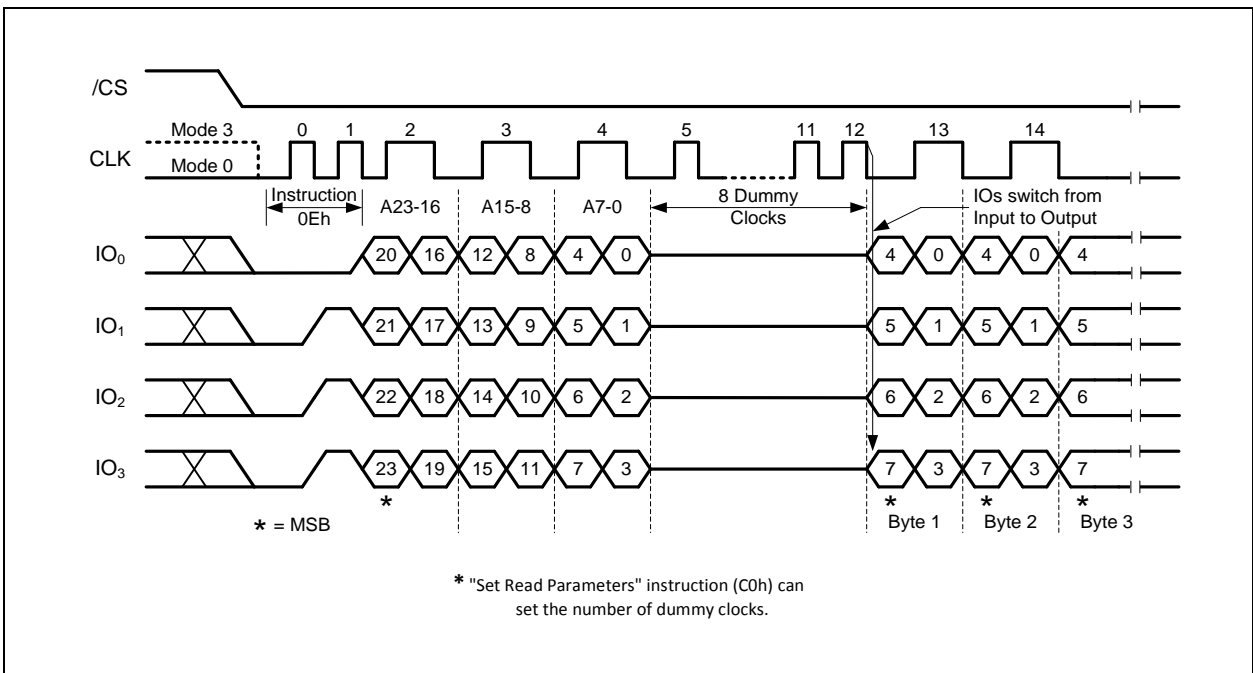


Figure 50. DTR Burst Read with Wrap Instruction (QPI Mode only)



8.2.39 Enter QPI Mode (38h)

The W25Q12PW support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of Winbond serial flash memories. See Instruction Set Table 1-3 for all supported SPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored and the device will remain in SPI mode.

See Instruction Set Table 3 for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

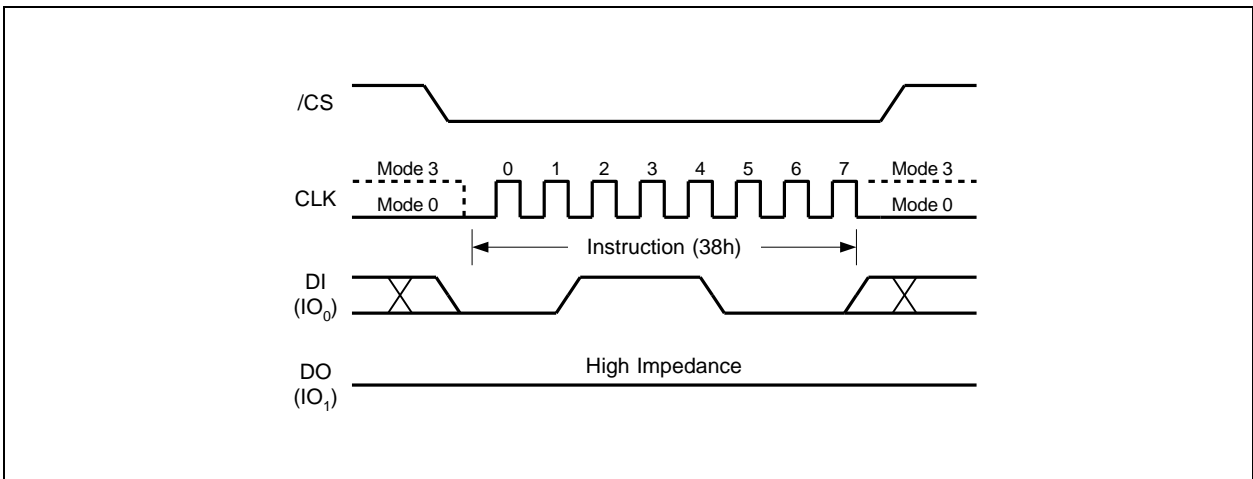


Figure 51. Enter QPI Instruction (SPI Mode only)



8.2.40 Exit QPI Mode (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

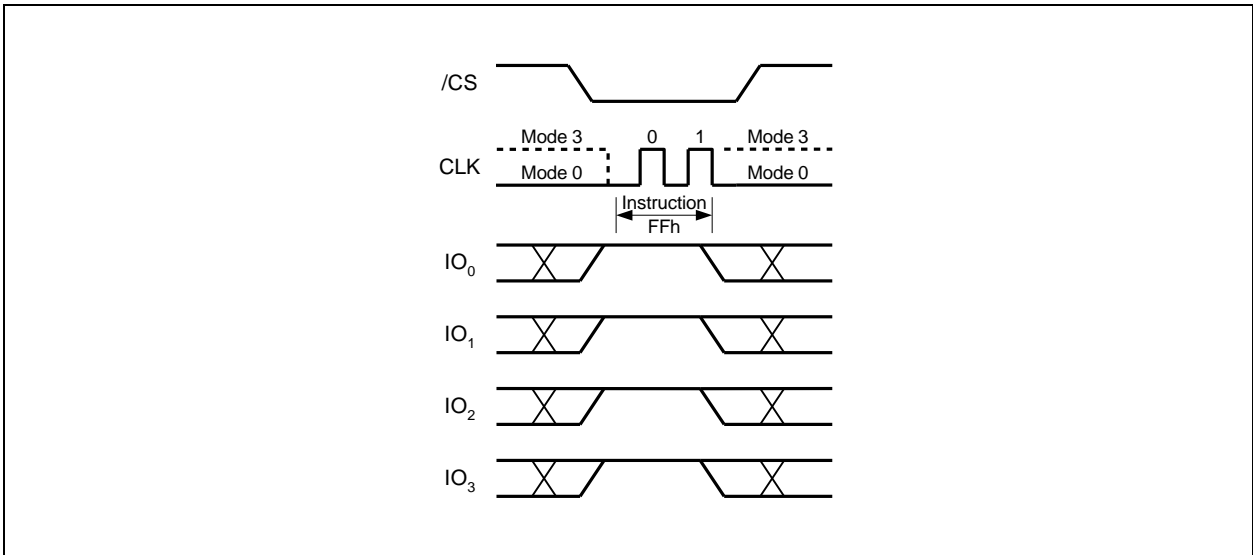


Figure 52. Exit QPI Instruction (QPI Mode only)



8.2.41 Enable Reset (66h) and Reset Device (99h)

Because small packages have a limited on the number of pins, the W25Q12PW provides a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated, and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), Read Command Bypass Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

“Enable Reset (66h)” and “Reset (99h)” instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately $t_{RST}=30\mu s$ to reset. During this period, no command will be accepted.

When “Enable Reset (66h)” and “Reset (99h)” instructions are issued in QPI, the device will switch to SPI.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when the Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in the Status Register before issuing the Reset command sequence.

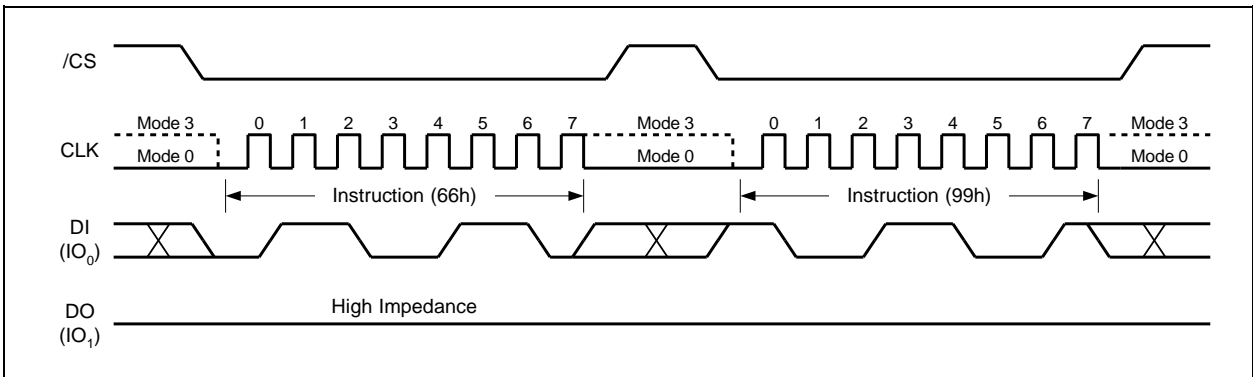


Figure 58a. Enable Reset and Reset Instruction Sequence (SPI Mode)

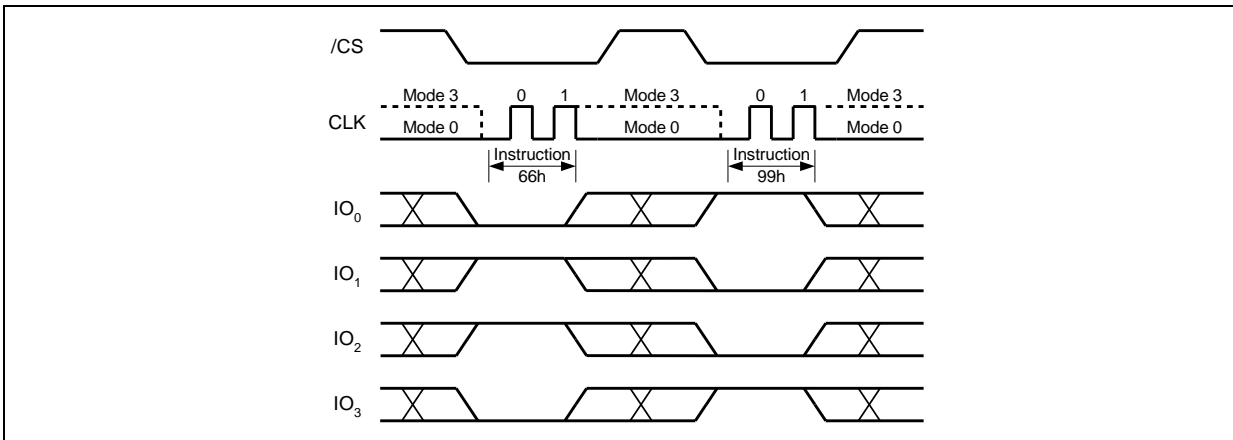


Figure 58b. Enable Reset and Reset Instruction Sequence (QPI Mode)



9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings ⁽¹⁾

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		-0.6 to 2.5	V
Voltage Applied to Any Pin	VIO	Relative to Ground	-0.6 to VCC+0.4	V
Transient Voltage on any Pin	V _{IO} T	<20nS Transient Relative to Ground	-2.0V to VCC+2.0V	V
Storage Temperature	TSTG		-65 to +150	°C
Lead Temperature	TLEAD		See Note ⁽²⁾	°C
Electrostatic Discharge Voltage	VESD	Human Body Model ⁽³⁾	-2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage ⁽¹⁾	VCC	F _R = 166MHz with 12-16T dummy F _R = 133MHz, f _R = 104MHz	1.65	1.95	V
Ambient Temperature, Operating	T _A	Industrial	-40	+85	°C

Note:

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.



9.3 Power-Up Power-Down Timing and Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	tVSL ⁽¹⁾	20		μs
Time Delay Before Write Instruction	tPUW ⁽¹⁾	5		ms
Write Inhibit Threshold Voltage	VWI ⁽¹⁾	1.0	1.4	V
The Minimum Duration For Ensuring Initialization Will Occur	tPWD ⁽¹⁾	100		μs
VCC Voltage Needed To Below V _{PWD} For Ensuring Initialization Will Occur	V _{PWD} ⁽¹⁾		0.8	V

Note:

1. These parameters are characterized only.

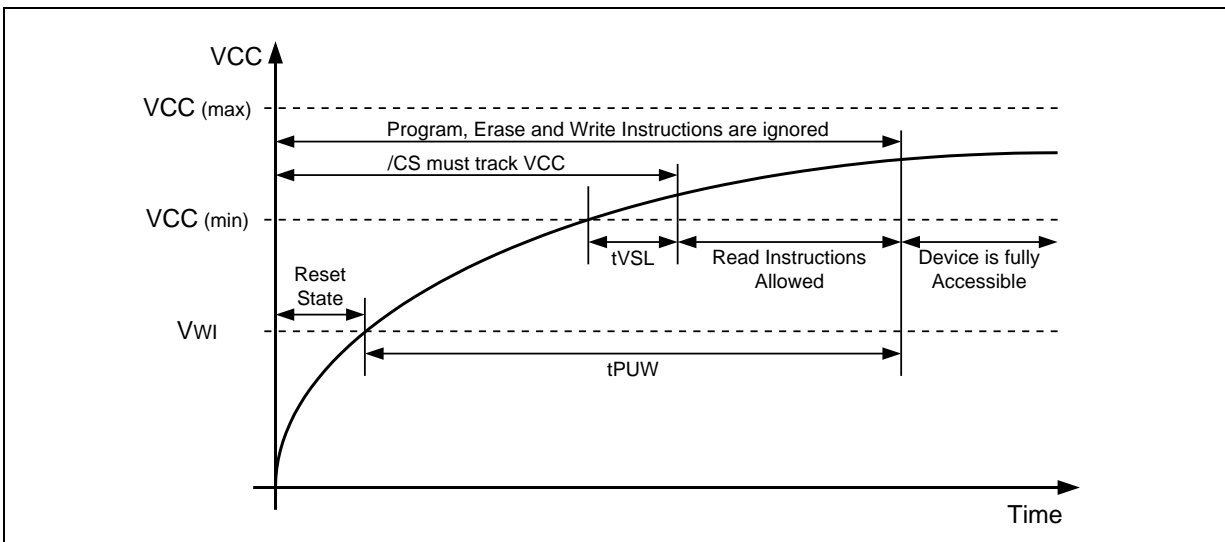


Figure 65a. Power-up Timing and Voltage Levels

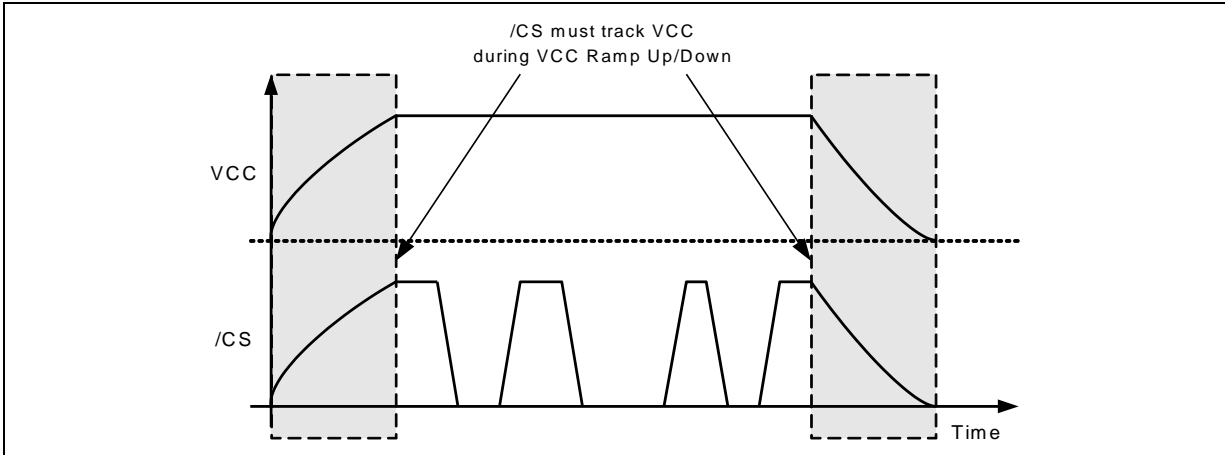


Figure 64b. Power-up, Power-Down Requirement

9.3.1 Power Cycle Requirement

For power cycle, the system must not initial the power-up sequence until Vcc drops down to V_{PVD} and keeps a t_{PVD} for device to initialize correctly.

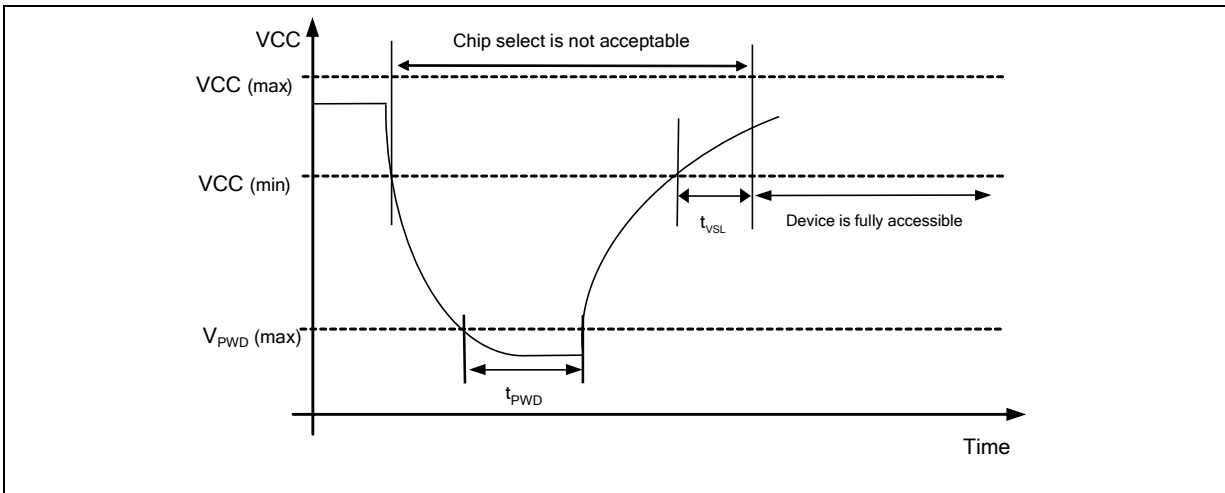


Figure 65c. Power Cycle Requirement

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9.4 DC Electrical Characteristics-

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C _{IN} ⁽¹⁾	V _{IN} = 0V ⁽¹⁾			6	pF
Output Capacitance	C _{out} ⁽¹⁾	V _{OUT} = 0V ⁽¹⁾			8	pF
Input Leakage	I _{LI}				±2	μA
I/O Leakage	I _{LO}				±2	μA
Standby Current	I _{CC1}	/CS = VCC, VIN = VSS or VCC		10	50	μA
Power-down Current	I _{CC2}	/CS = VCC, VIN = VSS or VCC		1	10	μA
Read Data / Dual /Quad 84MHz Current	I _{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		4	8	mA
Read Data / Dual /Quad 104MHz Current	I _{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		5	9	mA
Read Data / Dual /Quad 133MHz Current	I _{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		6	12	mA
Read Data / Dual /Quad 166MHz Current	I _{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		8	14	mA
Write Status Register Current	I _{CC4}	/CS = VCC		15	20	mA
Page Program Current ⁽²⁾	I _{CC5}	/CS = VCC		15	20	mA
Sector/Block Erase Current	I _{CC6}	/CS = VCC		15	20	mA
Current Chip Erase Read Current	I _{CC7}	/CS = VCC		15	20	mA
Input Low Voltage	V _{IL}		-0.5		VCC x 0.3	V
Input High Voltage	V _{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V _{OL}	I _{OL} = 100 μA			0.2	V
Output High Voltage	V _{OH}	I _{OH} = -100 μA	VCC - 0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V.
2. Checker Board Pattern.



9.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	CL		30	pF
Input Rise and Fall Times	TR, TF		5	ns
Input Pulse Voltages	VIN	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

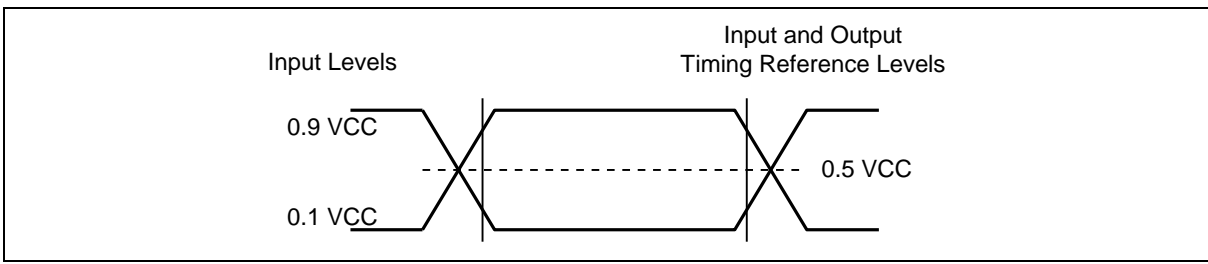


Figure 59. AC Measurement I/O Waveform

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9.6 AC Electrical Characteristics

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency with 12~16T dummy	F _R	f _{C1}	D.C.		166 ⁽⁶⁾	MHz
Clock frequency except for Read Data (03h) & DTR instructions	F _R	f _{C1}	D.C.		133 ⁽⁶⁾	MHz
Clock frequency DTR instructions	F _R	f _{C1}	D.C.		104 ⁽⁶⁾	MHz
Clock frequency for Read Data instruction (03h)	f _R		D.C.		104 ⁽⁶⁾	MHz
Clock High, Low Time for all instructions except for Read Data (03h)	t _{CLH} , t _{CLL} ⁽¹⁾		45% PC			ns
Clock High, Low Time for Read Data (03h) instruction	t _{CRLH} , t _{CRLL} ⁽¹⁾		45% PC			ns
Clock Rise Time peak to peak	t _{CLCH} ⁽²⁾		0.1			V/ns
Clock Fall Time peak to peak	t _{CHCL} ⁽²⁾		0.1			V/ns
/CS Active Setup Time relative to CLK	t _{SLCH}	t _{CSS}	4			ns
/CS Not Active Hold Time relative to CLK	t _{CHSL}		3			ns
Data In Setup Time	t _{DVCH}	t _{DSU}	1			ns
Data In Hold Time	t _{CHDX}	t _{DH}	2			ns
/CS Active Hold Time relative to CLK	t _{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t _{SHCH}		3			ns
/CS Deselect Time (for Read)	t _{SHSL1}	t _{CSH}	10			ns
/CS Deselect Time (for Erase or Program or Write)	t _{SHSL2}	t _{CSH}	50			ns
/CS Deselect Time (for program/erase) to /BUSY Low	t _{SHBL}				80	ns
/BUSY high to /CS Active	t _{BHSL}			0		ns
Output Disable Time	t _{SHQZ} ⁽²⁾	t _{DIS}			7	ns
Clock Low to Output Valid	t _{CLQV}	t _V			4.5	ns
Output Hold Time	t _{CLQX}	t _{HO}	1			ns
/HOLD Active Setup Time relative to CLK	t _{HLCH}		5			ns
/HOLD Active Hold Time relative to CLK	t _{CHHH}		5			ns

Continued – next page

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AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Not Active Setup Time relative to CLK	tHHCH		5			ns
/HOLD Not Active Hold Time relative to CLK	tCHHL		5			ns
/HOLD to Output Low-Z	tHHQX ⁽²⁾	tLZ			7	ns
/HOLD to Output High-Z	tHLQZ ⁽²⁾	tHZ			12	ns
Write Protect Setup Time Before /CS Low	tWHSL ⁽³⁾		20			ns
Write Protect Hold Time After /CS High	tSHWL ⁽³⁾		100			ns
/CS High to Power-down Mode	tDP ⁽²⁾				3	μs
/CS High to Standby Mode without ID Read	tRES1 ⁽²⁾				3	μs
/CS High to Standby Mode with ID Read	tRES2 ⁽²⁾				1.8	μs
/CS High to next Instruction after Suspend	tSUS ⁽²⁾				20	μs
/CS High to next Instruction after Reset	tRST ⁽²⁾				30	μs
Write Status Register Time	tW			1	15	ms
Page Program Time	tPP ⁽⁷⁾			0.12	1.5	ms
Sector Erase Time (4KB)	tSE			30	400	ms
Block Erase Time (32KB)	tBE ₁			90	800	ms
Block Erase Time (64KB)	tBE ₂			120	1,000	ms
Chip Erase Time	tCE			10	100	s
Data In Setup Time (DTR Only)	tDVCL		1			ns
Data In Hold Time (DTR Only)	tCLDX		2			ns
Clock Low to Output Valid (DTR Only)	tCHQV				4.5	ns
Output Hold Time (DTR Only)	tCHQX	tHO	1			ns

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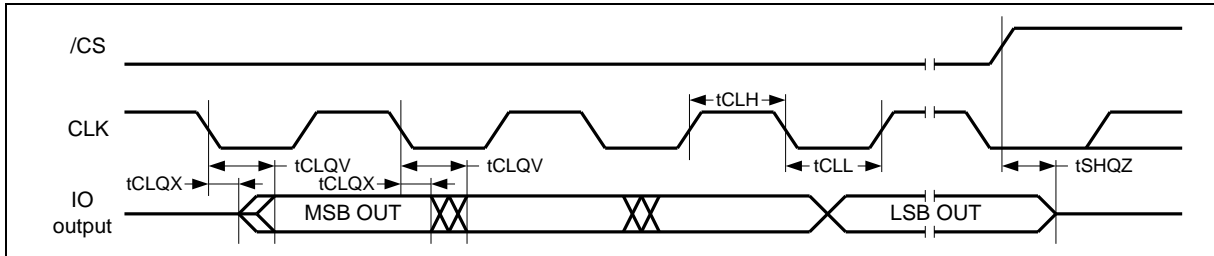


Notes:

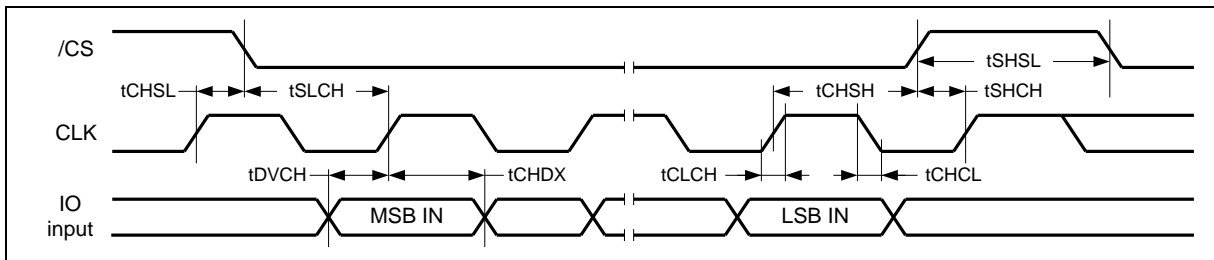
1. Clock high or Clock low must be more than or equal to 45%Pc. $P_c = 1/f_c(\text{max})$.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP=1.
4. It's possible to reset the device with shorter t_{RESET} (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.
5. Tested on sample basis and specified through design and characterization data. $T_A = 25^\circ \text{C}$, $V_{CC} = 3.0\text{V}$, 25% driver strength.
6. 4-bytes address alignment for QPI/Quad Read
7. With 55h/AAh pattern



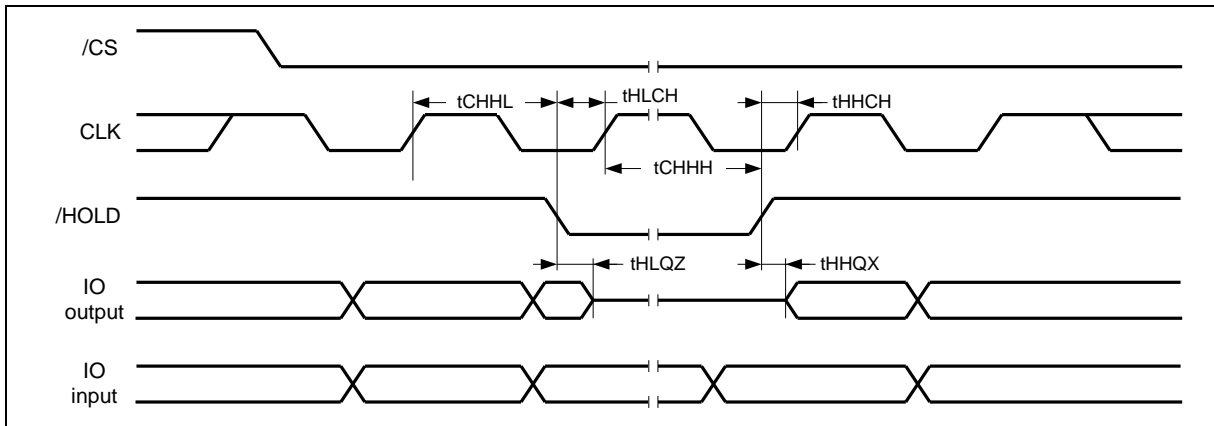
9.7 Serial Output Timing



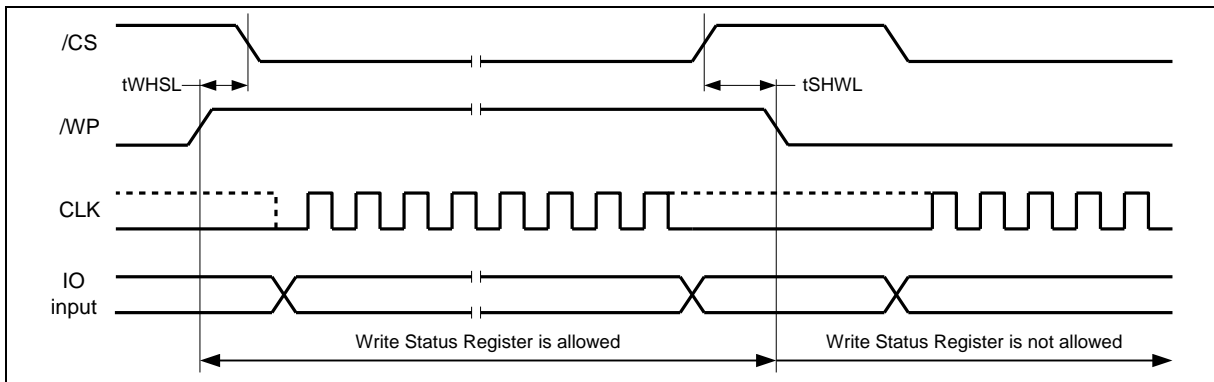
9.8 Serial Input Timing



9.9 /HOLD Timing



9.10 /WP Timing

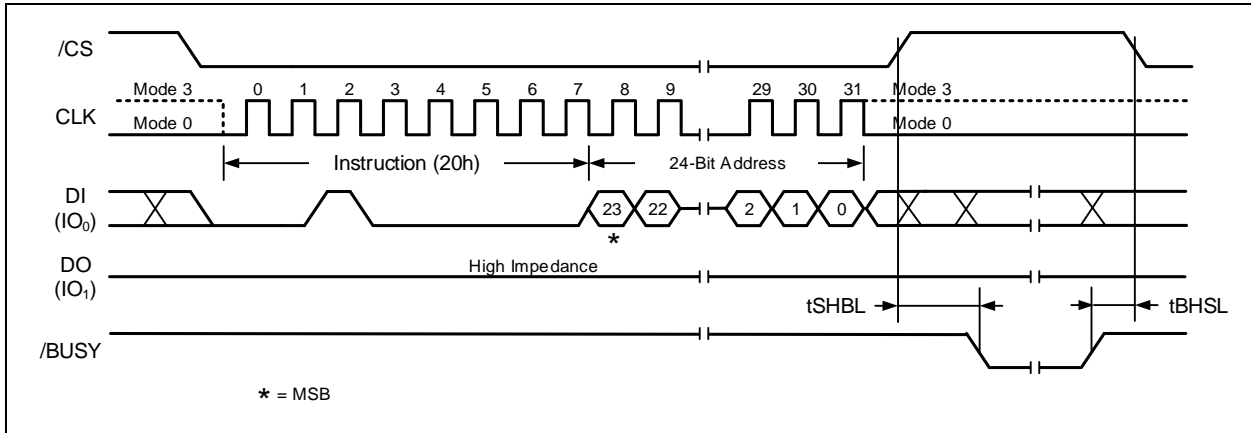


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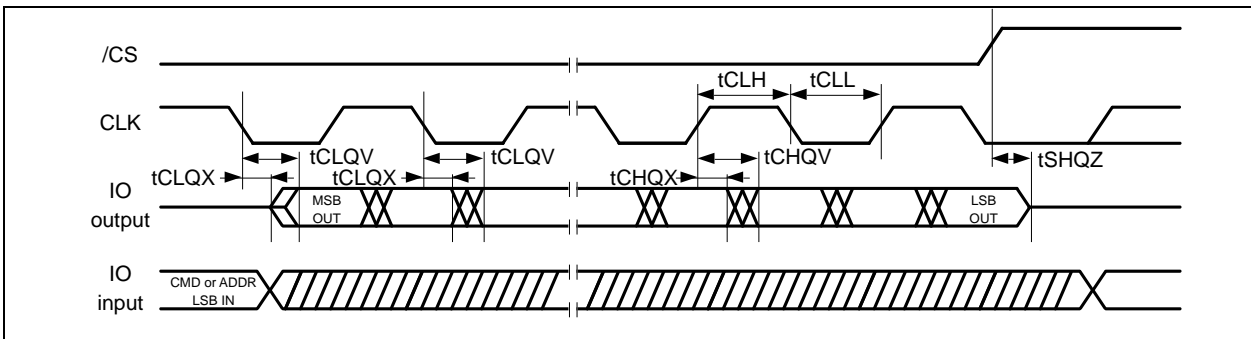


9.11 /BUSY Timing

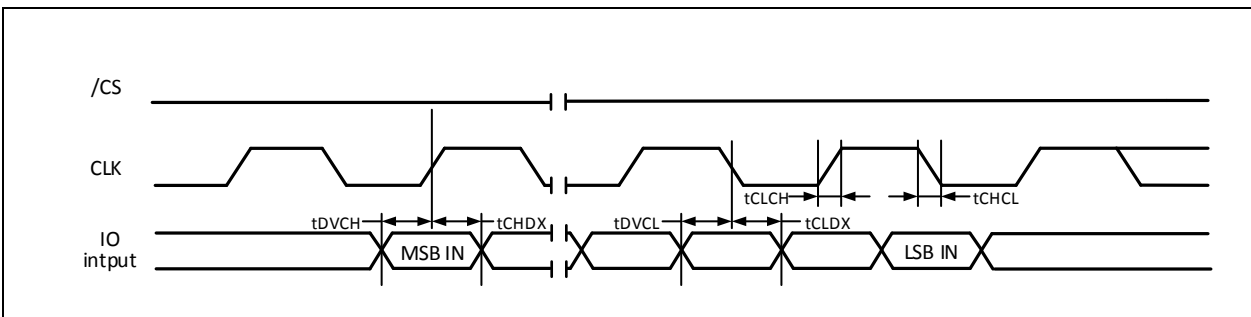
The following timing diagram illustrates /BUSY signal behavior during Sector Erase (20h) instruction. All other **Erase and Program** instructions have similar timing relationship between /CS and /BUSY.



9.12 DTR Output Timing



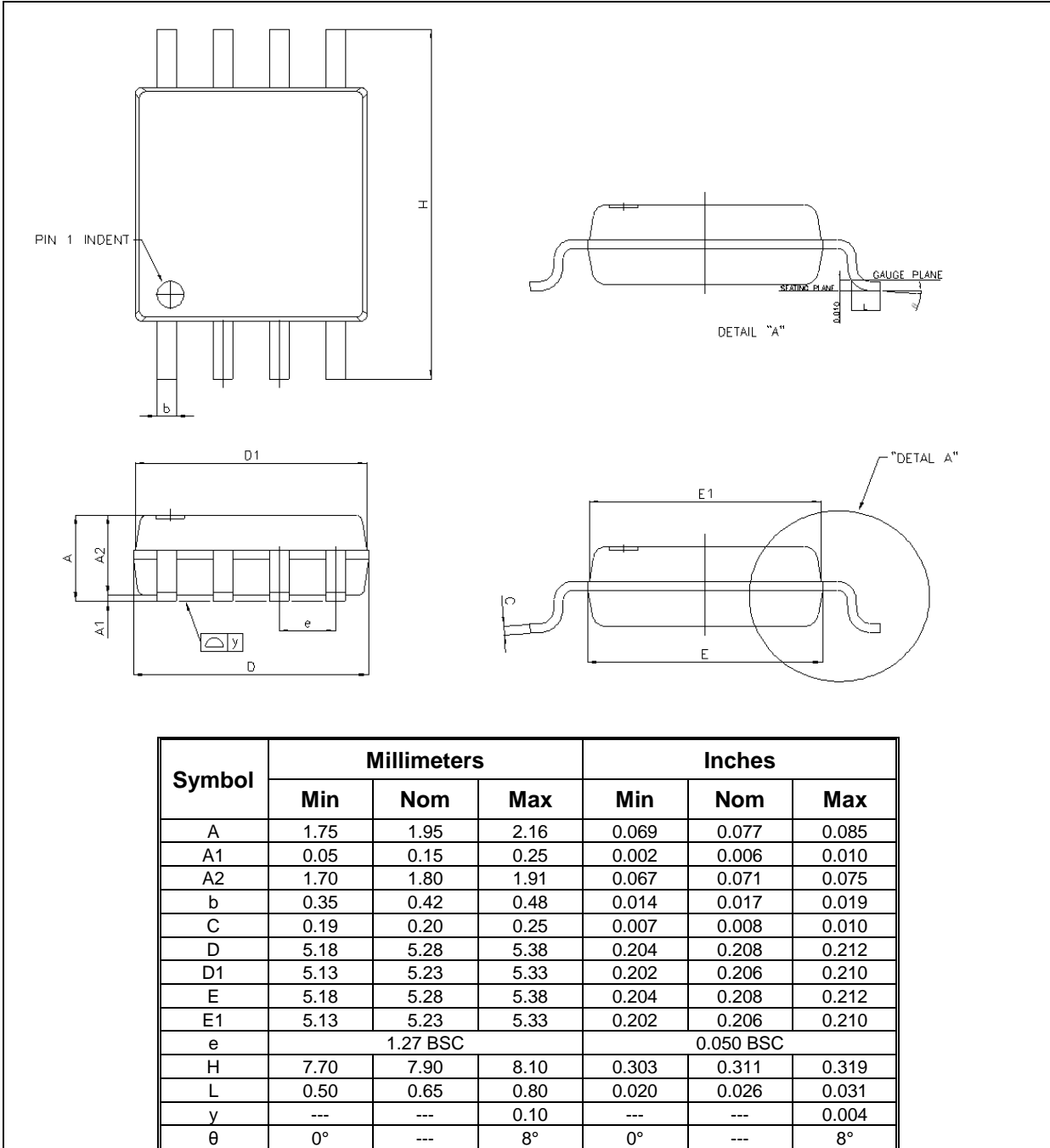
9.13 DTR Input Timing





10. PACKAGE SPECIFICATIONS

10.1 8-Pin SOP 208-mil (Package Code CS/SS)

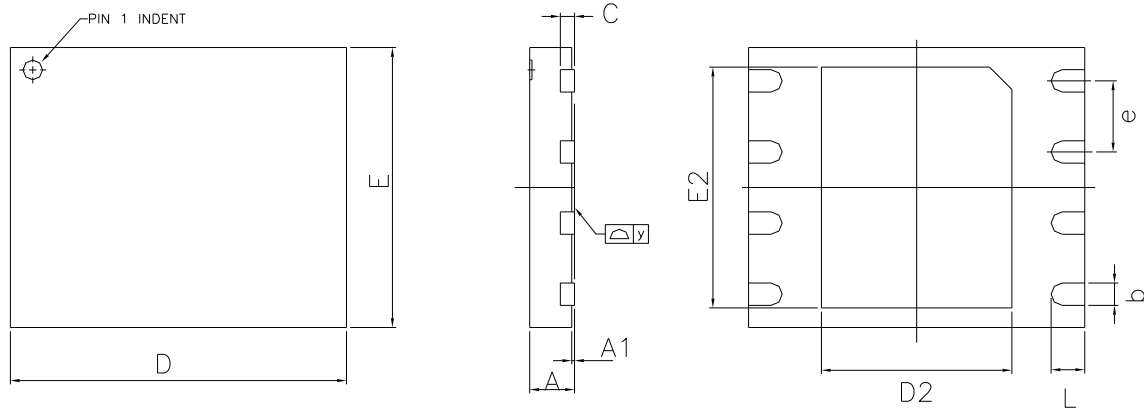


Note:

1. Control dimensions are in millimeter.
2. Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)

10.2 8-Pad WSON 6x5-mm (Package Code CP/ZP)

W25Q12PW-DTR



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF	---	---	0.008 REF	---
D	5.90	6.00	6.10	0.232	0.236	0.240
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	4.25	4.30	4.35	0.167	0.169	0.171
e	1.27 BSC			0.050 BSC		
L	0.55	0.60	0.65	0.022	0.024	0.026
y	0.00	---	0.075	0.000	---	0.003

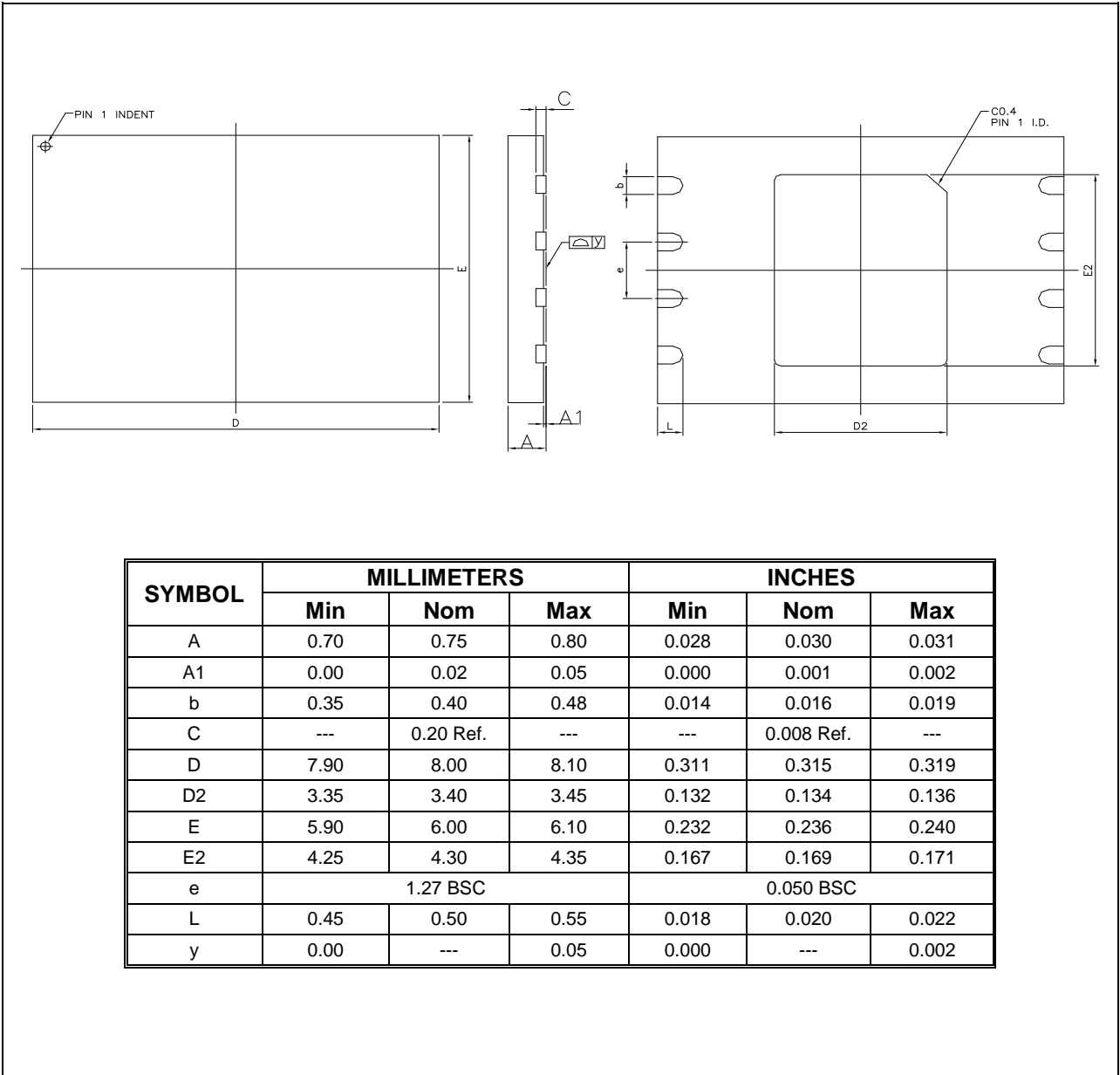
Note:

The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.

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10.3 8-Pad WSON 8x6-mm (Package Code CE/ZE)



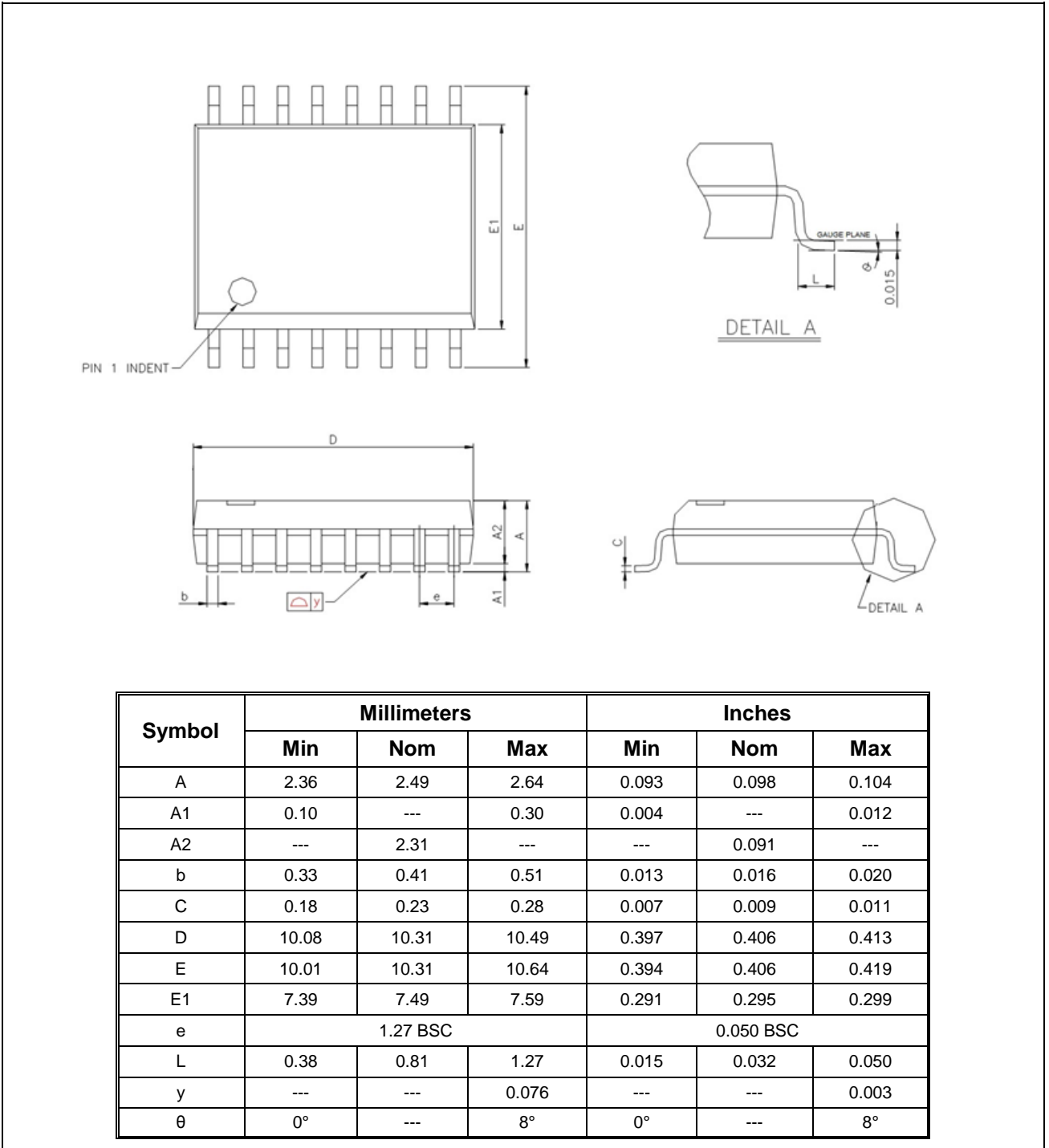
Note:

The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.

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10.4 16-Pin SOP 300-mil (Package Code CF/SF)

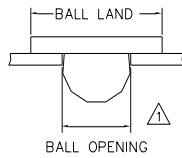
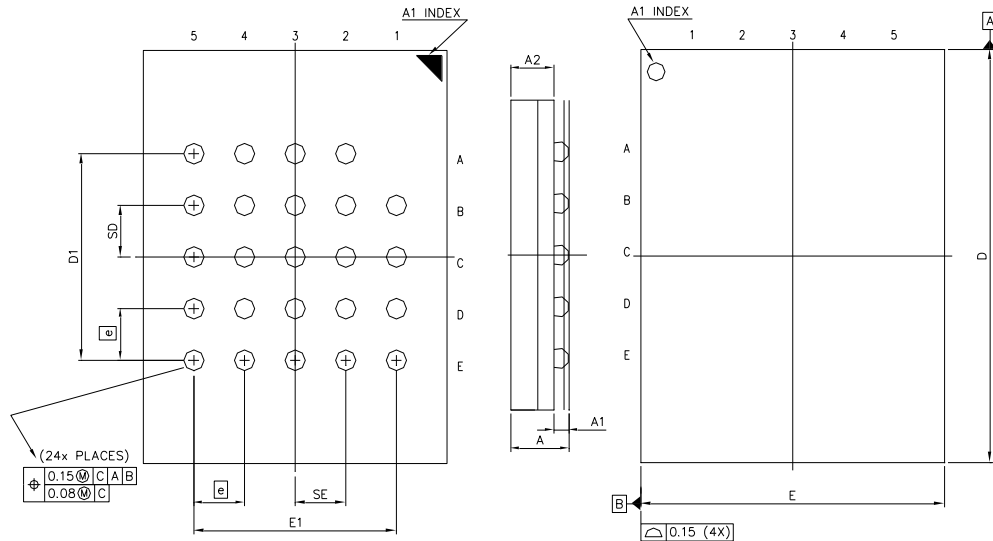


Note: Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)

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10.5 24-Ball TFBGA 8x6-mm (Package Code CB, 5x5-1 ball array)



Note:

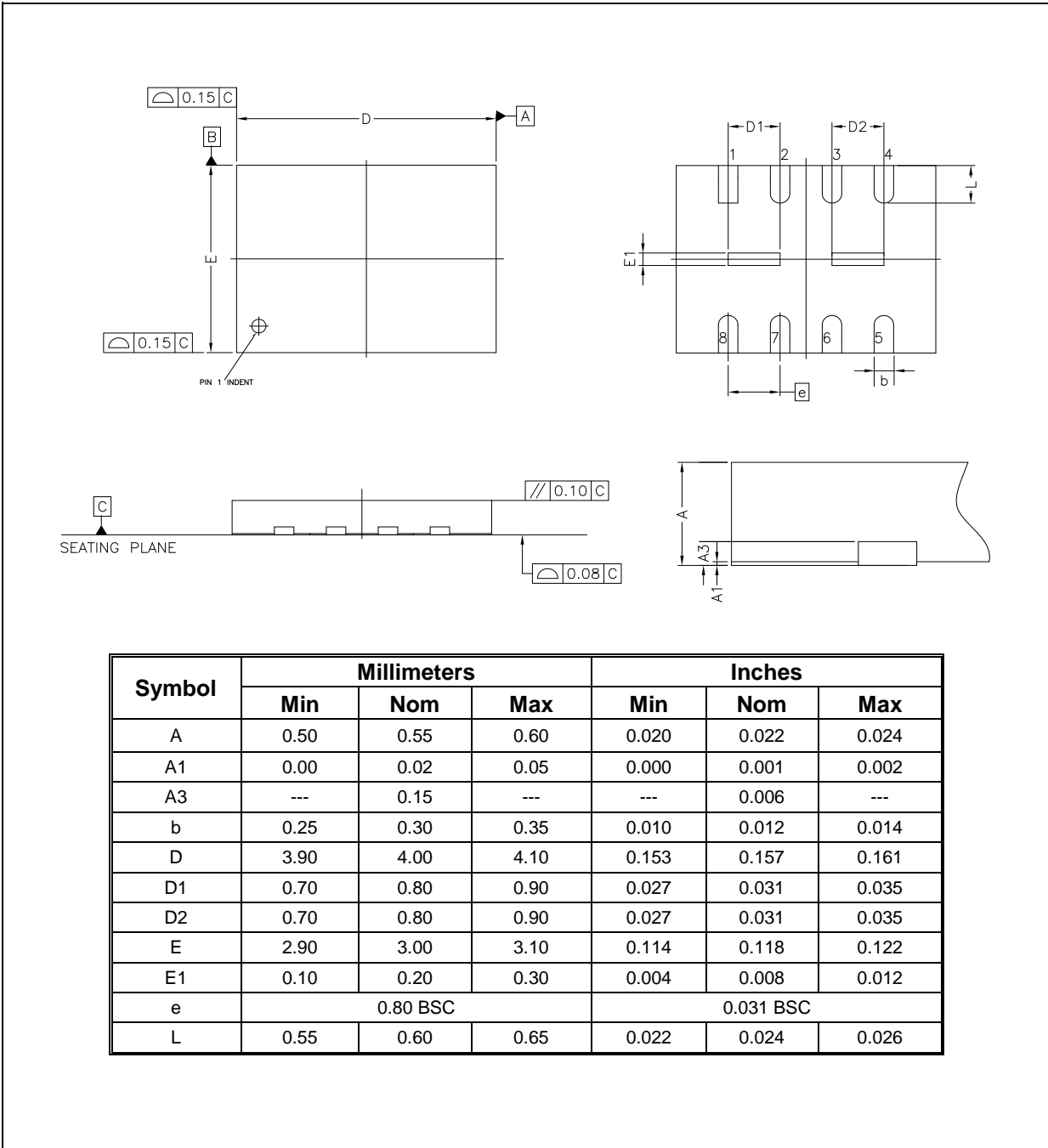
Ball land: 0.45mm. Ball Opening: 0.35mm
PCB ball land suggested \leq 0.35mm

Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.20	---	---	0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	---	0.85	---	---	0.033	---
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	4.00 BSC			0.157 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.00 BSC			0.157 BSC		
SE	1.00 TYP			0.039 TYP		
SD	1.00 TYP			0.039 TYP		
e	1.00 BSC			0.039 BSC		

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10.6 8-Pad USON 4x3-mm (Package Code UU)



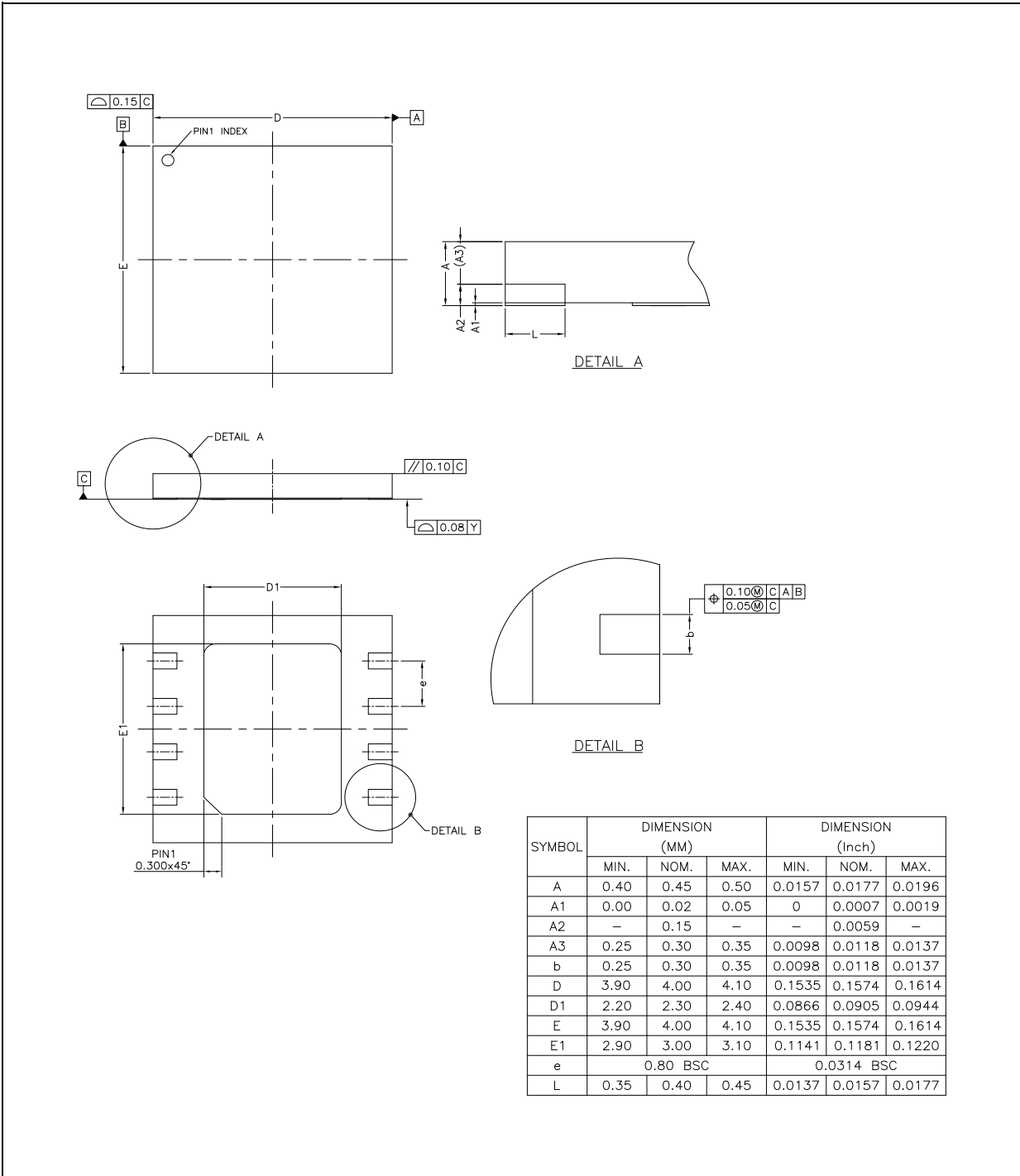
Note:

The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.

W25Q12PW-DTR



10.7 8-Pad XSON 4x4x0.45-mm (Package Code XG)

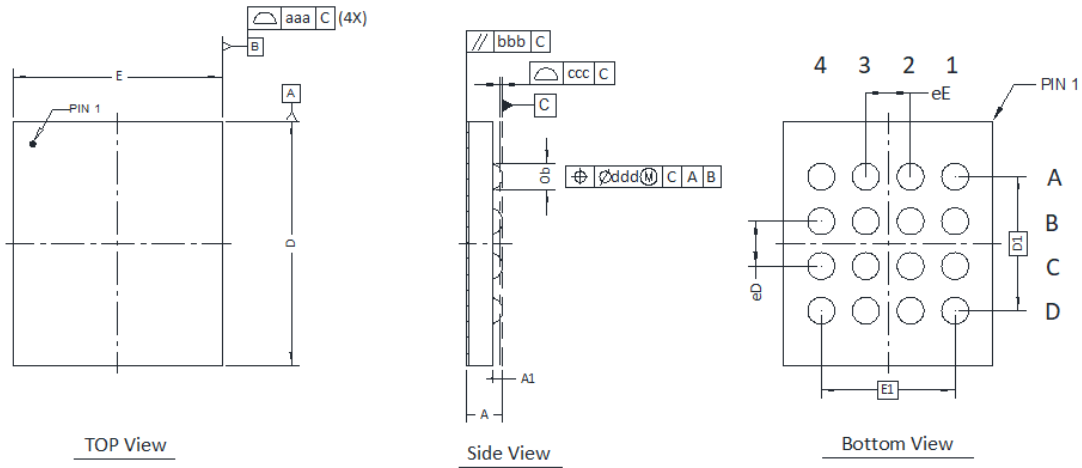


W25Q12PW-DTR



10.8 16-Ball WLCSP (Package Code BY)

Ball pitch: 0.50mm, with backside coating



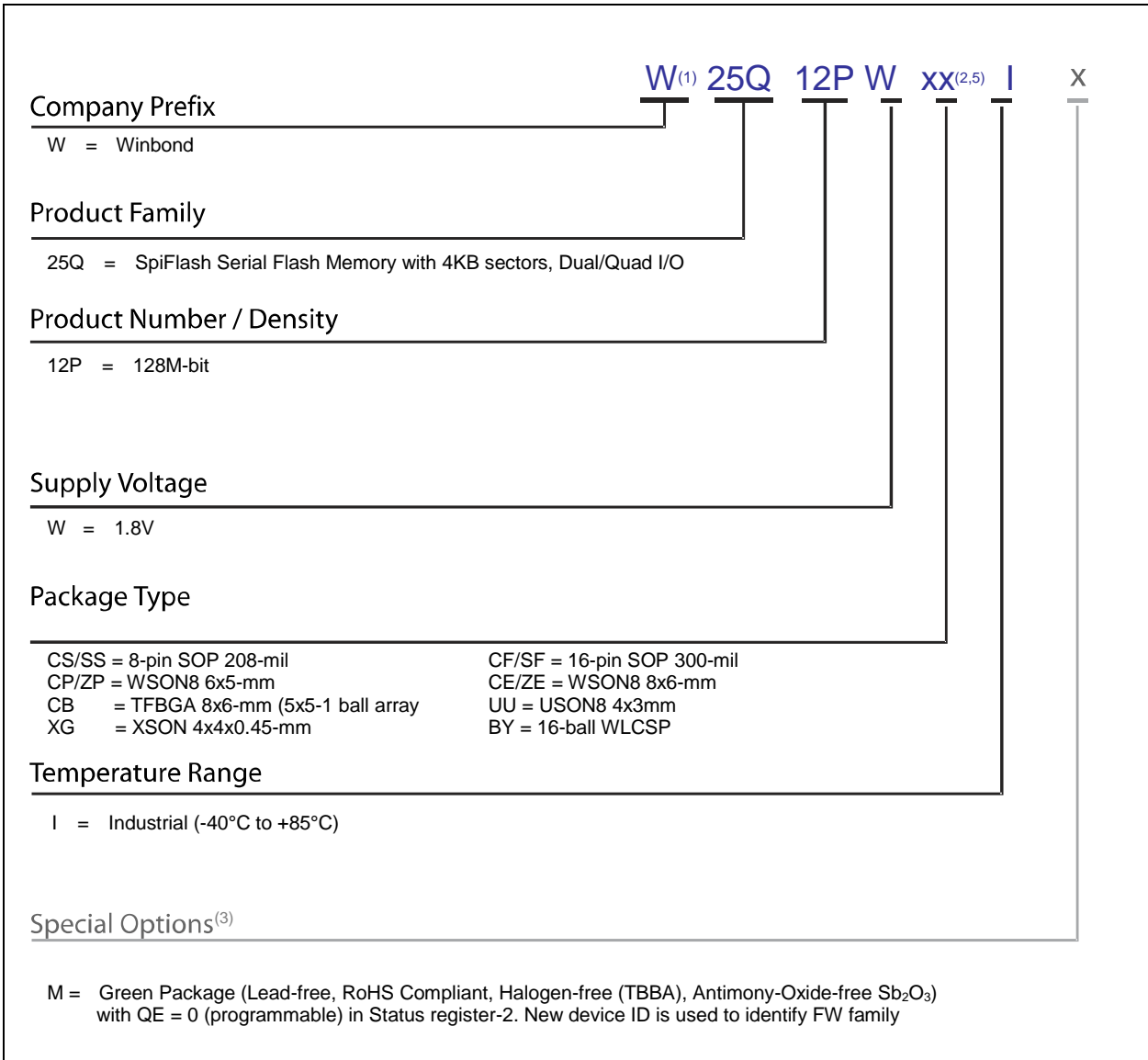
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.362	0.405	0.448	0.014	0.016	0.018
A1	0.100	0.115	0.130	0.004	0.005	0.005
D1	1.500 BSC			0.059 BSC		
E1	1.500 BSC			0.059 BSC		
eD	0.500 BSC			0.020 BSC		
eE	0.500 BSC			0.020 BSC		
b	0.240	0.300	0.360	0.009	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ccc	0.050			0.002		
ddd	0.150			0.006		

Note: Dimension b is measured at the maximum solder bump diameter, parallel to primary datum C. Control dimensions are in millimeter.

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11. ORDERING INFORMATION⁽⁶⁾



Notes:

1. The "W" prefix is not included on the part marking.
2. Only the 2nd letter is used for the part marking; WSON package type ZP & ZE are not used for the part marking.
3. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T) or Tray (shape S), when placing orders.
4. /HOLD function is disabled to support Standard, Dual and Quad I/O without user setting.
5. All devices are in compliance of RoHs, Halogen free, TSCA, and REACH.

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11.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25Q12PW SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 10-digit number.

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
CS SOP-8 208-mil	128M-bit	W25Q12PWCSIM	25Q12PWCSIM
CF SOP-16 300mil	128M-bit	W25Q12PWCFIM	25Q12PWCFIM
CP WSON-8 6x5-mm	128M-bit	W25Q12PWCPIM	Q12PWCPIM
CE WSON-8 8x6mm	128M-bit	W25Q12PWCEIM	25Q12PWCEIM
CB TFBGA-24 8x6mm (5x5-1 Ball Array)	128M-bit	W25Q12PWCBIM	25Q12PWCBIM
SS SOIC-8 208-mil	128M-bit	W25Q12PWSSIM	25Q12PWSIM
SF SOP16 300-mil	128M-bit	W25Q12PWSFIM	25Q12PWFIM
ZP WSON-8 6x5-mm	128M-bit	W25Q12PWZPIM	25Q12PWIM
ZE WSON-8 8x6-mm	128M-bit	W25Q12PWZEIM	25Q12PWIM
UU USON-8 4x3mm	128M-bit	W25Q12PWUUIM	Q12PWUUIM
XG XSON-8 4x4x0.45-mm	128M-bit	W25Q12PWXGIM	Q12PWXGIM
BY 16-ball WLCSP	128M-bit	W25Q12PWBYIM	Q12PW BYIM ●XXXX ⁽²⁾

Note:

1. These package types are special order, please contact Winbond for more information.
2. yyww: year/ week.

11.2 Initial delivery status

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The memory array is delivered in the erased state, where all data bits are set to '1' (FFh per byte). This covers all Part Numbers listed in Section "Valid Part Numbers and Top Side Marking".



12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	09/21/2023 ~ 10/13/2023	10 102	New Create Preliminary Updated BUSY pin with pull-up driver Updated Part No. table
B	02/22/2024	90	Removed preliminary Added tBHSL timing
C	03/11/2024	100	Updated ddd value as 0.150-mm/0.006-inch
D	09/03/2024	0 26 88	Added Serial NOR Flash Added byte 9 in Instruction Set Table 2 Updated Note tested samples at 1.8v
E	07/17/2025	7,26,28 94,97 6,7,98,101,105 106 7	Added Buffer Mode Added DTR AC timing and input/output timing Updated SOIC to SOP and add JEDEC note Updated SOIC to SOP Modified Notice (2) and added (3) to clarify that 16-byte alignment is required for qualification and supports data reliability and endurance
F	10/27/2025	8-10,99-102	Modified Part No. from SS,SF,ZP,ZE,TB to CS,CF,CP,CE,CB
G	01/06/2026	92	Updated ICC1 from 20/60 to 10/50µA
H	02/11/2026	8-9,99-102	Added Package code SS,SF,ZP,ZE
I1	04/22/2026	10 36,66 110	Updated TFBGA with /BUSY ball in A5 Added 31h/11h in 75h/50h description Added Initial delivery status

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