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Copy-back operation flow for W25N QspiNAND and W35N OctalNAND

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## **Purpose**

The purpose of this application note is to explain how to realize Copy-back operation on W25N QspiNAND and W35N OctalNAND.

## **Introduction**

Copy-back operations make it possible to transfer data within a device from one page to another using the data buffer. This is particularly useful for block management and wear leveling.

The Copy-back operation is a two-step process consisting of a Page Data Read (13h) and a Program Execute (10h) command. If the data of the whole page including the spare area contains correctable bit error, the first step Page Data Read (13h) correct the bit error when ECC-E bit in Status Register-2 is 1 (On-chip ECC is enabled).

In the next step, Program Execute (10h), the page data with corrected bit error can be programmed to another page address. During this process, if ECC-E=1, On-chip ECC performs parity calculation on the page data in which the bit error has been corrected, and the result is programmed in the spare area.

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### Target devices

The copy-back operation described in this application note is available for the following devices.

- W25N QspiNAND series
  - W25N512GVxxx (512Mb, 3.3V, STR 104MHz)
  - W25N512GWxxx (512Mb, 1.8V, STR 104MHz)
  - W25N01GWxxxx (1Gb, 1.8V, STR 104MHz)
  - W25M02GWxxxx<sup>1</sup> (2Gb, 1.8V, STR 104MHz)
  - W25N02KVxxxx<sup>2</sup> (2Gb, 3.3V, STR 104MHz)
  - W25N04KVxxxx<sup>1,2</sup> (4Gb, 3.3V, STR 104MHz)
- W25N High Performance QspiNAND series
  - W25N01JWxxxx (1Gb, 1.8V, STR 166MHz / DTR 83MHz)
  - W25N02JWxxxx<sup>1</sup> (2Gb, 1.8V, STR 166MHz / DTR 83MHz)
- W35N OctalNAND series
  - W35N01JWxxxx (1Gb, 1.8V, STR 166MHz / DTR 120MHz)
  - W35N02JWxxxx<sup>1</sup> (2Gb, 1.8V, STR 166MHz / DTR 120MHz)
  - W35N04JWxxxx<sup>1</sup> (4Gb, 1.8V, STR 166MHz / DTR 120MHz)

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<sup>1</sup> This product is consist of multiple dies. The program destination address by copy-back can be specified on the same Die as the read address.

<sup>2</sup> This product is consist of two planes. The program destination address by copy-back can be specified on the same plane as the read address.

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**Operation flow for Copy-back with ECC-E=1 (On-chip ECC is enabled)**

Copy-back operation with ECC-E=1 can be executed by the procedure shown in Figure 1 below. As a premise, it is assumed that the page address "yyy" of the program destination is in Erase state.

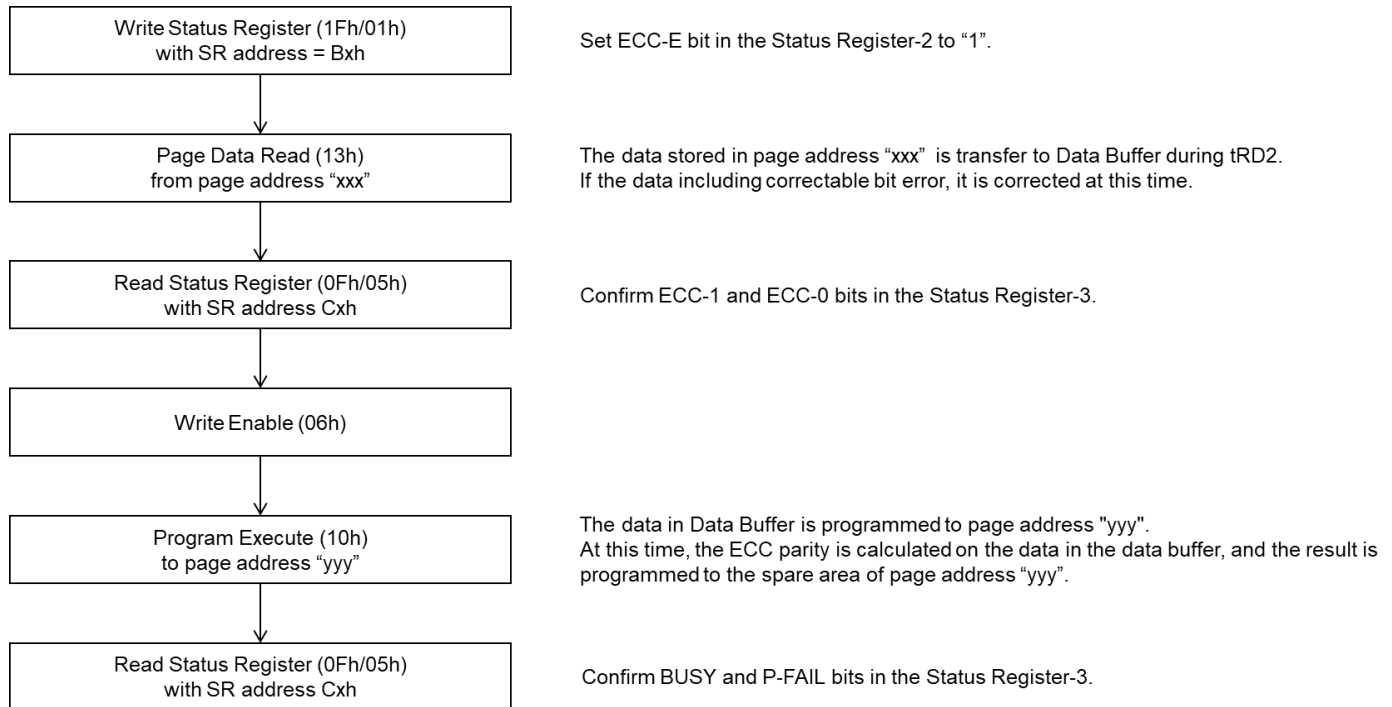


Figure 1 Operation flow for Copy-back with ECC-E=1 (On-chip ECC is enabled)

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**Operation flow for Copy-back with ECC-E=0 (On-chip ECC is disabled)**

Copy-back operation with ECC-E=0 can be executed by the procedure shown in Figure 2 below. As a premise, it is assumed that the page address "yyy" of the program destination is in Erase state.

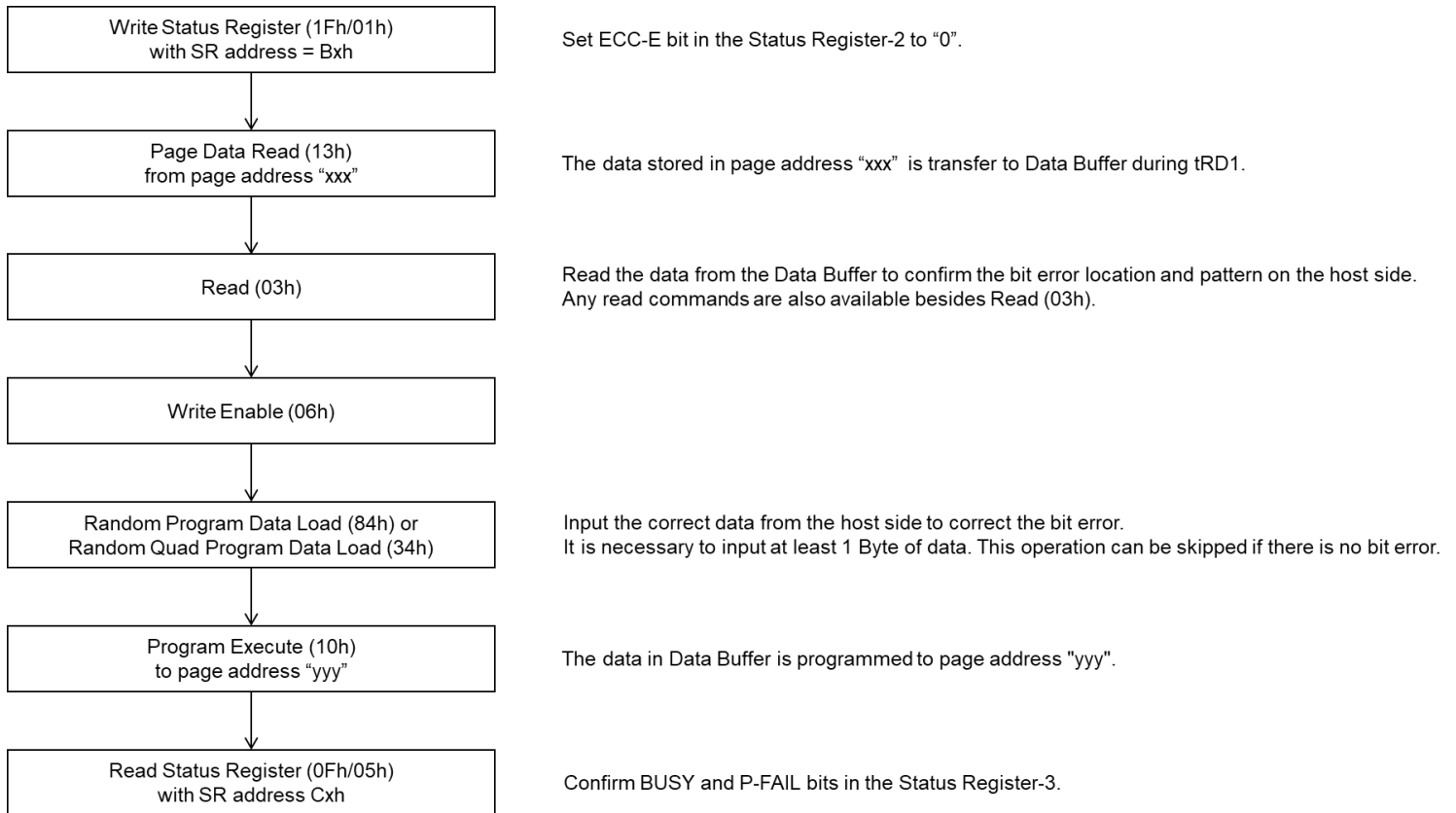


Figure 2 Operation flow for Copy-back with ECC-E=0 (On-chip ECC is disabled)

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**Revision History**

Version	Date	Page	Description
1.0	7/22/2020	NA	New create
1.1	8/3/2020	2	Updated the note for multiple die products Added the note for W25N02KV and W25N04KV

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