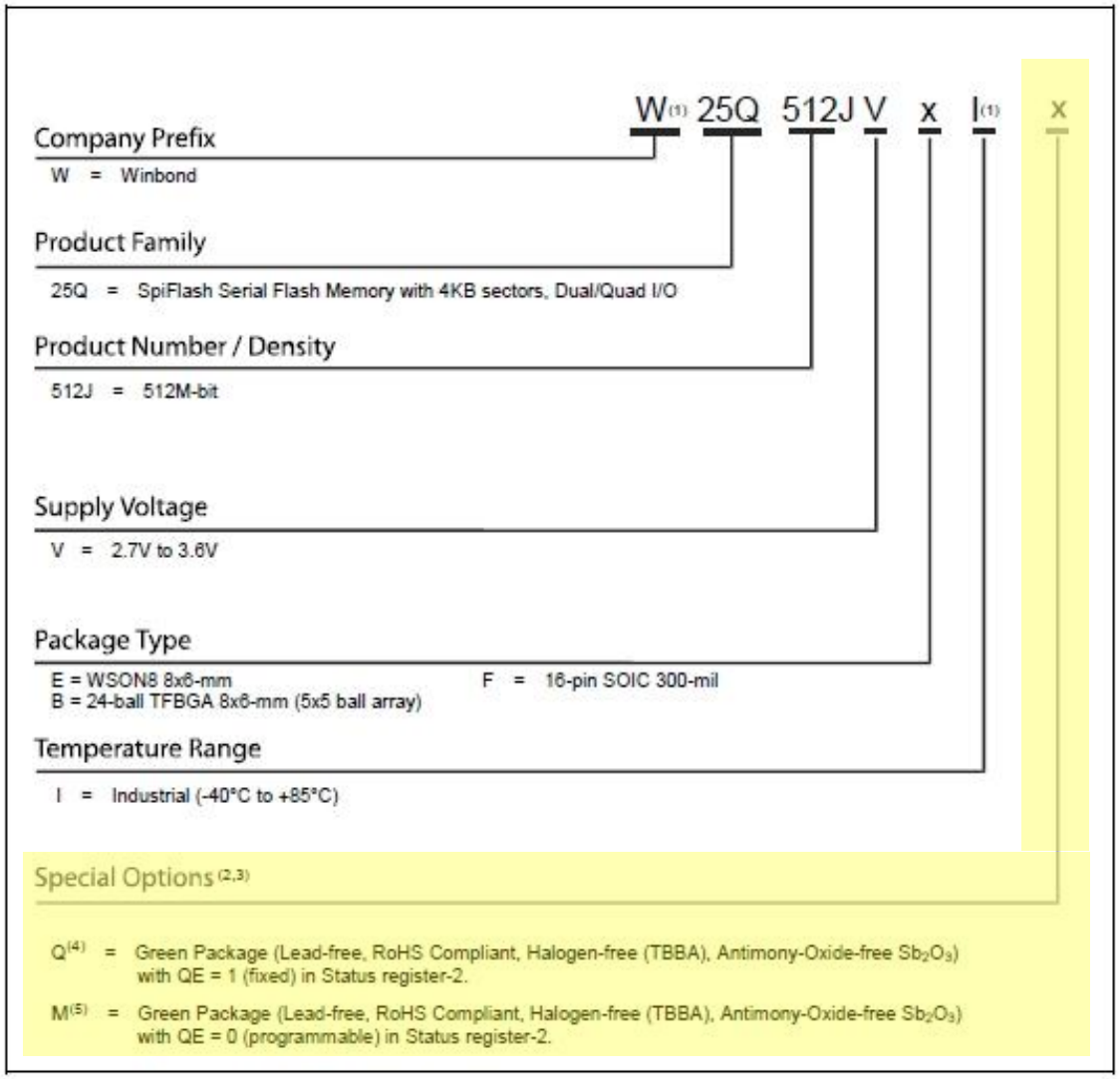
Introduction

There are two special hardware options within the Winbond W25QxxJV/W25QxxJW families of SpiFlash which can be identified by the Q or M suffix in the ordering part number. Not to be confused with the “Q” in the W25**Q** “Quad Capable” family name, this “Q/M” is an option suffix used to identify “Quad Preset” feature. An example of the part numbering scheme and where to locate the Q/M suffix is shown in the diagram below.

Although the features and functionality of both families are very similar, the fundamental difference between the two variants is that Q-parts can support Quad SPI at initial power up in addition to the single or dual bit SPI while M-parts only supports single or dual bit SPI at initial power up . This document outlines their differences and explains how to select, configure and utilize specific functions on each part to avoid confusion.



Feature Comparison

	Q Option	M Option
Modes	Can be boot in single, dual, or quad bit mode.	Can be boot in single or dual bit mode.
QE bit	Not changeable, fixed as “1”.	Programmable. Both volatile and non-volatile version can be set to “1” after boot.
QPI	Not supported.	Supported.
DTR Mode	Not supported.	Supported.
/RESET	No /RESET function in SOIC-8 package.	/RESET is pin shared with IO3 or as a separate pin in higher pin count packages.
/HOLD	No /HOLD function.	/HOLD available at boot. This pin functions as IO3 if set to Quad mode (QE=1) after boot.
Continuous Read	Not supported.	Supported.

Product Selection

Based on the above feature comparison table, the selection between Q and M parts becomes much more straightforward.

Select Q-parts if:

- Quad mode is required at boot-up.
- QPI mode, DTR mode, HOLD function, and Continuous Read are not required.

Select M-parts if:

- Power up in standard 1 bit or 2 bit SPI mode.
- QPI mode, DTR mode, or Continuous Read is required.
- HOLD or RESET functions are required.
- Enabling and disabling of QE bit is required. For such application, user should only use the volatile version to switch between QE enable and QE disable. Note that once the non-volatile version is set, it overrides the volatile version.

Q Option Specific Operations

Since the Quad Enable (QE bit) is not programmable and factory fixed as "1", this means Quad SPI is always available even at power-up. The Q option specific operations are described in the following sections.

Package Pins

The following table describes how shared package pins are used during each mode.

Pin Name	Descriptions
DI or IO0	In Standard mode, this is used as DI. In Dual or Quad mode, this pin is used as IO0.
DO or IO1	In Standard mode, this is used as DO. In Dual or Quad mode, this pin is used as IO1.
/WP or IO2	/WP is a hardware control pin to prevent the Status Register from being written. Since Status Register can only be written in Standard or Dual mode, while IO2 is only used during Quad instructions, these two signals can coexist. Only during Quad instructions, this signal is used as IO2.
/HOLD or /RESET or IO3	For SOIC-8 package where these 3 signals share the same package pin, this pin is always used as IO3. /HOLD and /RESET functions are not supported. On the larger SOIC-16 or TFPGA packages, where there is a dedicated /RESET pin, Hardware reset function is supported through this pin. The /HOLD and IO3 pin is always used as IO3 and /HOLD function is not supported.

Enable/Disable Quad SPI Mode

If users try to enable/disable Quad mode by writing a 1/0 into the Status Register QE bit, the write instruction will execute normally but there is no effect to the device operation. Any subsequent read of the QE bit will always return a 1.

Trying To Enter QPI Mode

Even as Quad Enable is fixed as 1, the issuing of **Enter QPI (38h)** instruction will be ignored and has no effect on the interface. The device will remain in SPI mode.

DTR Read Instructions

All unsupported instructions are either not implemented or not tested and might result in unexpected behavior. Users should not use unsupported instruction codes.

Treatment of /HOLD pin

/HOLD pin is always used as Quad mode IO3, users should never treat /HOLD as a control signal for hold functionality.

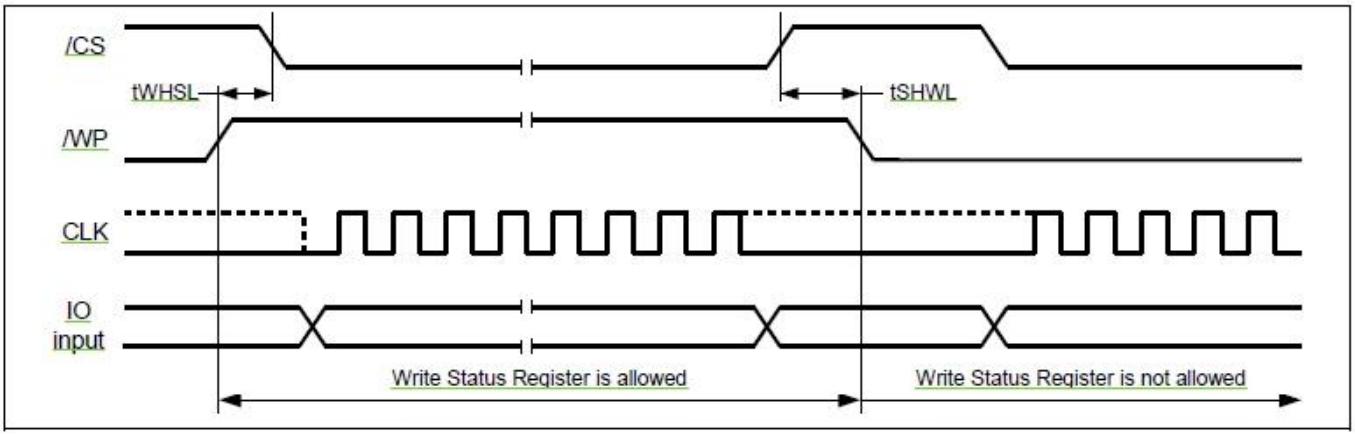
Using Write Protect /WP Signal

As described in the Package Pins section, even though Write Protect (/WP) shares the same signal pin as Quad mode IO2, both features can coexist when Quad mode is enabled. This is because Status Register can only be written in Standard or Dual SPI mode which means /WP is only used as Write Protect during non-Quad instructions. During Quad instructions, /WP become IO2 signal.

/WP is a hardware mechanism used in conjunction with Status Register Protect (SRP), and Status Register Lock (SRL) to prevent any update to the Status Register. The following table describes the five different protection modes.

SRL	SRP	/WP	Status Register	**Descriptions**
0	**0**	**X**	**Software Protection**	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	**1**	**0**	**Hardware Protected**	When /WP pin is low, the Status Register is locked and cannot be written to.
0	**1**	**1**	**Hardware Unprotected**	When /WP pin is high, the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	**X**	**X**	**Power-Supply Lock-down**	Status Register is protected and cannot be written to again until the next power cycle.
1	**X**	**X**	**One Time Program**	Status Register is permanently protected and cannot be written to. (enabled by adding prefix command AAh, 55h)

In order to use /WP hardware protected mode, SRL and SRP are to be set as 0 and 1 respectively. There is also a setup and hold time requirement between /WP and /CS in order for /WP to not block write instructions to the Status Register. The timing diagram on the following page illustrates the /WP signal timing requirements during Standard and Dual SPI mode.



Description	Symbol	Spec			Unit
		Min	Typ	Max	
Write Protect Setup Time Before /CS Low	**tWHSL**	20			ns
Write Protect Hold Time After /CS High	**tSHWL**	100			ns

Note: These timings are for reference only. For the exact AC timing requirements for your device, please consult the datasheet.

Continuous Read (Read Command Bypass Mode)

Continuous Read (Read Command Bypass Mode) is not supported.

M Option Specific Operations

Quad Enable (QE bit) is volatile/non-volatile writable and default as “0”, this means Quad SPI is not enabled during power-up. To enable Quad SPI, user has to perform either a volatile or a non-volatile write to set the Statue Register QE bit to “1”.

Package Pins

The following table describes how shared package pins are used during each mode.

Pin Name	Descriptions
DI or IO0	In Standard mode, this is used as DI. In Dual or Quad mode, this pin is used as IO0.
DO or IO1	In Standard mode, this is used as DO. In Dual or Quad mode, this pin is used as IO1.
/WP or IO2	/WP is a hardware control pin to prevent the Status Register from being written. Since Status Register can only be written in Standard or Dual mode, while IO2 is only used during Quad instructions, these two signals can coexist. Only during Quad instructions, this signal is used as IO2.
/HOLD or /RESET or IO3	These 3 signals share the same package pin, if Quad mode is not enabled, the function of this pin is controlled by the HOLD/RST bit in the Status Register. By default HOLD/RST=0, this pin functions as /HOLD. If HOLD/RST is set to 1, this pin becomes /RESET. If Quad mode is enabled, this pin act as IO3, /HOLD and /RESET functions are disabled. On the larger SOIC-16 or TFPGA packages, there is a dedicated /RESET pin, hardware reset function can be controlled through this pin.

Enable/Disable Quad SPI Mode

M option parts are factory default as Quad mode disabled. To enable Quad SPI operations, perform a volatile or non-volatile Status Register write to set the QE bit to 1.

By using a volatile write, user has the flexibility to disable Quad SPI quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the non-volatile Status Register bits. To write the volatile QE bit, a **Volatile Status Register Write Enable (50h)** instruction must be issued prior to a **Write Status Register (01h)** instruction.

If the application prefers to have Quad SPI always enabled, a non-volatile write is recommended. To write the non-volatile QE bit, make sure WEL is enabled by issuing a **Write Enable (06h)** instruction, then set QE to 1 by using a **Write Status Register (01h)** instruction.

Note that a write to the non-volatile QE-bit overrides the value in the volatile version of the QE-bit.

Enter/Exit QPI Mode

Quad Peripheral Interface (QPI) utilizes all four IO pins to input the instruction code, reducing instruction overhead and improve system performance.

To enter QPI mode, make sure QE bit is set to 1, then issue a **Enter QPI (38h)** to switch the device from Standard/Dual/Quad SPI to QPI. When the device is in QPI mode, QE bit will remain set. A **Write Status Register (01h)** command in QPI mode cannot change QE bit from a 1 to a 0.

To exit QPI mode, issue a **Exit QPI (FFh)** instruction.

DTR Read Instructions

Double Transfer Rate (DTR) Read instructions are supported in Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

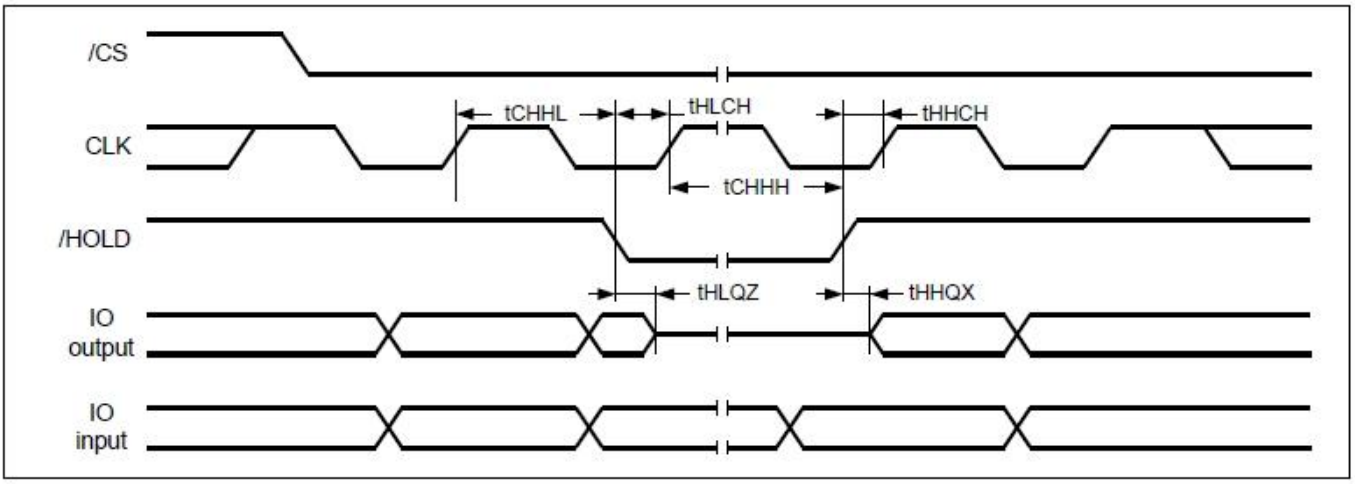
DTR instructions include

- **DTR Fast Read (0Dh)**
- **DTR Fast Read Dual I/O (BDh)**
- **DTR Fast Read Quad I/O (EDh)**
- **DTR Fast Read Wrap (0Eh)**

Treatment of /HOLD pin

By default, both QE and HOLD/RST bits in the Status Register are 0. This means Quad operations and RESET are disabled and this pin is used as /HOLD control. Note that on larger packages, a separate /RESET pin is available for hardware reset control.

The /HOLD function can be useful in cases where the SPI data and clock signals are shared with other devices. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where the bus is available again. The following timing diagram illustrates the timing requirement for /HOLD activation and deactivation.



Description	Symbol	Spec			Unit
		Min	Typ	Max	
/HOLD Active Setup Time relative to CLK	**tHLCH**	5			ns
/HOLD Active Hold Time relative to CLK	**tCHHH**	5			ns
/HOLD Not Active Setup Time relative to CLK	**tHHCH**	5			ns
/HOLD Not Active Hold Time relative to CLK	**tCHHL**	5			ns
/HOLD to Output Low-Z	**tHHQX**			8	ns
/HOLD to Output High-Z	**tHLQZ**			12	ns

Note: These timings are for reference only. For the exact AC timing requirements for your device, please consult the datasheet.

Another option is to use this signal as /RESET control. After boot-up, with QE default as 0, write a 1 to the HOLD/RST bit in the Status Register will assign this pin as /RESET control.

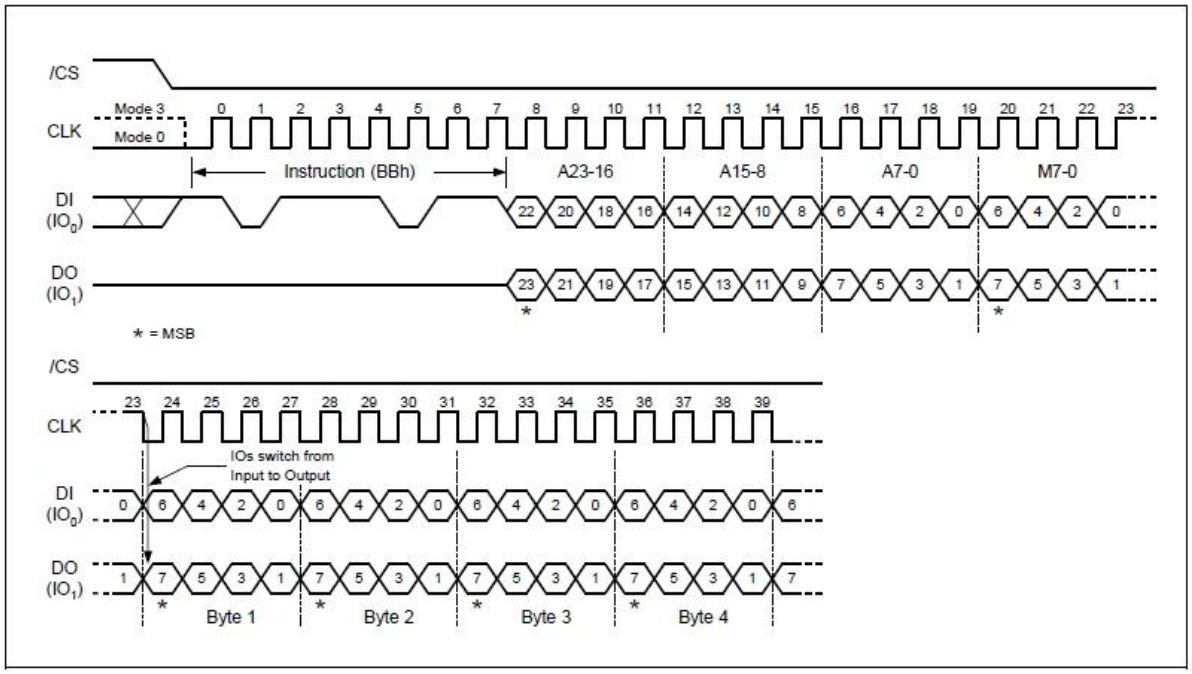
However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1 to enable Quad instructions, /HOLD and /RESET functions are disabled and this pin acts as a dedicated data I/O pin IO3.

Using Write Protect /WP Signal

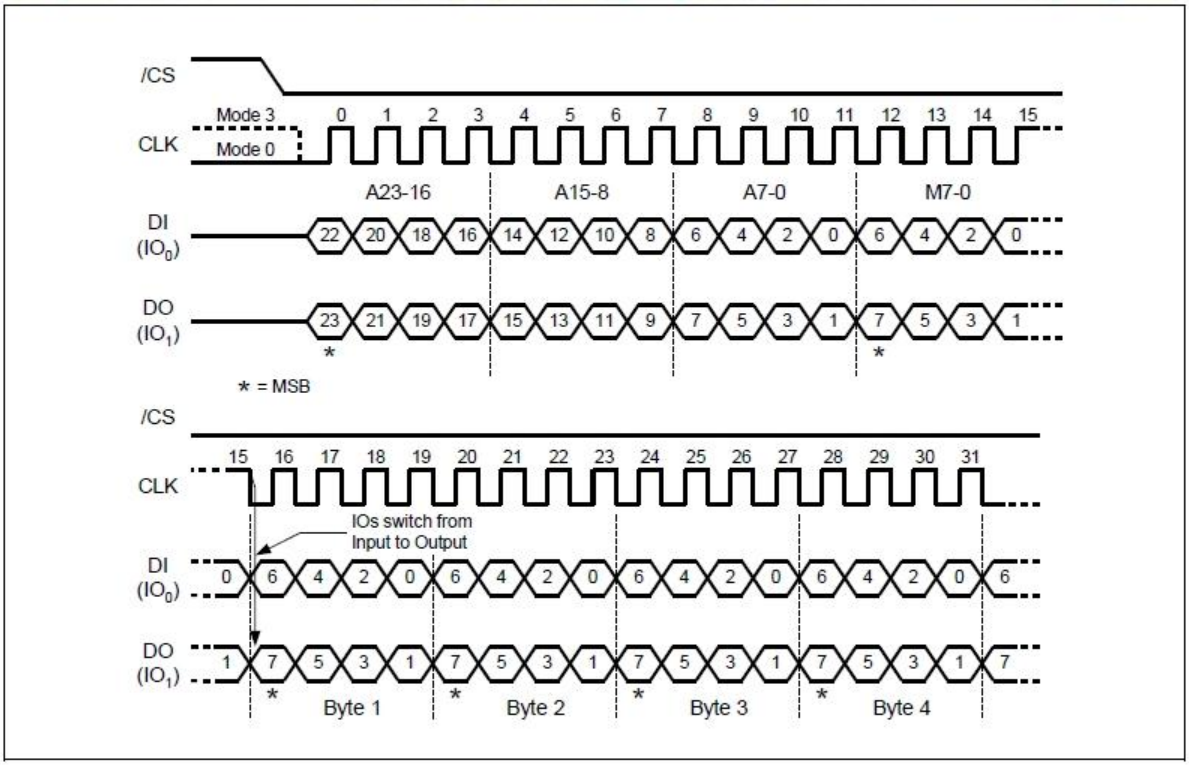
By default, QE is disabled which means /WP pin act as hardware Write Protect control signal. When Quad operation is enabled by setting the QE bit in the Status Register to 1, the behavior of the /WP signal is the same as Q option parts. Refer to the Q option section for usage and timing.

Continuous Read (Read Command Bypass Mode)

Continuous Read which should be better described as the Read Command Bypass Mode allows for efficient memory access eliminating the command code of consecutive read instructions. By setting the “Continuous Read” or “Read Command Bypass Mode” bits (M5-4) to [1,0] after the input Address bits (A23-0), as shown in the following timing diagram, the next Fast Read instruction (after /CS is raised and then lowered) does not require the sending of the Fast Read instruction code. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If M5-4 = [1,1], then the Read instruction code is required for the next instruction sequence.



First Command with Instruction Code and M5-4 = [1,0]



Next Command without Instruction Code

Reference

For the complete specification of both the Q and M option devices, please refer to the appropriate device datasheets.

Revision History

Version	Date	Page	Description
1.0	06/14/2020	NA	Original
1.1	07/09/2020	1	Clarify the difference between W25Q vs Q/M suffix.
		2,6	Updated Option M non-volatile QE-bit description.
		9	Update timing table with correct units and labels.

Trademarks

Important Notice