Migration Guide from SPI NOR to SPI NAND

1. Spec Comparison

Serial Flash Memory Comparison		SPI NOR(W25Q256JW)	SPI NAND(W25N01GW)
Technology		58nm	46nm
VCC		1.65 ~ 1.95V	1.65 ~ 1.95V
Package Types		SOP16 WSON 8x6mm BGA (6x4,5x5)	WSON 8x6mm BGA (6x4,5x5)
Page Program Size		256B	**2,048B**
Erase Granularity		Uniform 4/32/64KB	Uniform **128KB**
UID / OTP		64-Bit Unique ID 3x256Byte OTP	2,048-Byte Unique ID 2,048-Byte Parameter 10x2,048Byte OTP
JEDEC ID		EF6019h	EFBA21h
AC PARAMETERS			
Fast Read Speed	**FR**	Fast Read 80~104MHz	Fast Read 80~104MHz
		other cmds 104MHz	other cmds 104MHz
Page Program Time	**tPP**	0.7 / 3ms	0.25 / 0.7ms
4KB Sector Erase Time	**tSE**	50 / 400ms	NA
32KB Block Erase Time	**tBE1**	120 / 1,600ms	NA
64KB Block Erase Time	**tBE2**	150 / 2,000ms	NA
128KB Block Erase Time	**tBE**	NA	**2 / 10ms**
Chip Erase Time	**tCE**	80 / 400s	**2 / 10s**
DC PARAMETERS			
Read Current	**ICC rd**	20mA (104MHz)	25 / 35mA (104MHz)
Program/Erase Current	**ICC P/E**	20 / 25mA	25 / 35mA
Standby Current	**ICC stdby**	10 / 60µA	10 / 50µA

2. Operation Guide

2.1 Status Registers Sequence

Serial Flash Memory Comparison	SPI NOR(W25Q256JW)		SPI NAND(W25N01GW)		
Data Input Output	**Byte 1(Input)**	**Byte 2(output)**	**Byte 1(Input)**	**Byte 2(Input)**	**Byte 3(output)**
Clock Number	**(0 – 7)**	**(8 – 15)**	**(0 – 7)**	**(8 – 15)**	**(16 – 23)**
Read Status Register-1	**05h**	(S7-S0)	**05h / 0Fh**	**Axh**	(S7-S0)
Write Status Register-1	**01h**	(S7-S0)	**01h / 1Fh**	**Axh**	(S7-S0)
Read Status Register-2	**35h**	(S15-S8)	**05h / 0Fh**	**Bxh**	(S15-S8)
Write Status Register-2	**31h**	(S15-S8)	**01h / 1Fh**	**Bxh**	(S15-S8)
Read Status Register-3	**15h**	(S23-S16)	**05h / 0Fh**	**Cxh**	(S23-S16)

Write Status Register-3	**11h**	(S23-S16)	**01h / 1Fh**	**Cxh**	(S23-S16)

2.2 Status Registers Content

Serial Flash Comparison	**SPI NOR(W25Q256JW)**								**SPI NAND(W25N01GW)**							
Bits	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
Status Register-1	SRP0	SEC	TB	BP 2	BP 1	BP0	WE L	BUS Y	SRP 0	BP3	BP2	BP1	BP0	TB	WP-E	SRP1
Status Register-2	SUS	CMP	LB3	LB 2	LB 1	(R)	QE	SRP1	OTP -L	OTP -E	SR1-L	ECC -E	BUF	(R)	(R)	(R)
Status Register-3	HOLD /RST	DRV 1	DRV 0	(R)	(R)	WPS	(R)	(R)	(R)	LUT -F	ECC -1	ECC -0	P-FAIL	E-FAIL	WEL	BUSY

*. See the datasheets for detail usage.

2.3 Read Data Sequence

2.3.1 SPI NOR(W25Q256JW):

Read Data (03h): **03h** → 24bit Address → Data out
Read Data (13h): **13h** → 32bit Address → Data out
Fast Read (0Bh): **0Bh** → 24bit Address → 8bit Dummy → Data out
Fast Read (0Ch): **0Ch** → 32bit Address → 8bit Dummy → Data out
Fast Read Dual Output (3Bh): **3Bh** → 32/24bit Address → 8bit Dummy → Data out by 2
Fast Read Quad Output (6Bh): **6Bh** → 32/24bit Address → 8bit Dummy → Data out by 4
Fast Read Dual I/O (BBh): **BBh** → 32/24bit Address by 2 → 8bit Dummy by 2 → Data out by 2
Fast Read Quad I/O (EBh): **EBh** → 32/24bit Address by 4 → 8bit Dummy by 4 → Data out by 4

2.3.2 SPI NAND(W25N01GW):

Page Data Read(13h): **13h** → 8bit Dummy → 16bit Page Address
(Page Data Read(13h) command has to be executed for loading a specific page address)

*. Continuous Mode (data out from byte 0 to continuously)
Read Data (03h): **03h** → 24bit Dummy → Data out
Fast Read (0Bh): **0Bh** → 32bit Dummy → Data out
Fast Read (0Ch): **0Ch** → 40bit Dummy → Data out
Fast Read Dual Output (3Bh): **3Bh** → 32bit Dummy → Data out by 2
Fast Read Dual Output (3Ch): **3Ch** → 40bit Dummy → Data out by 2
Fast Read Quad Output (6Bh): **6Bh** → 32bit Dummy → Data out by 4
Fast Read Quad Output (6Ch): **6Ch** → 40bit Dummy → Data out by 4
Fast Read Dual I/O (BBh): **BBh** → 32bit Dummy by 2(16clocks) → Data out by 2
Fast Read Dual I/O (BCh): **BCh** → 40bit Dummy by 2(20clocks) → Data out by 2
Fast Read Quad I/O (EBh): **EBh** → 48bit Dummy by 4(12clocks) → Data out by 4
Fast Read Quad I/O (ECh): **ECh** → 56bit Dummy by 4(14clocks) → Data out by 4

*. Buffer Mode (data out up to end of page)
Read Data (03h): **03h** → 16bit Column Address → 8bit Dummy → Data out
Fast Read (0Bh): **0Bh** → 16bit Column Address → 8bit Dummy → Data out
Fast Read (0Ch): **0Ch** → 16bit Column Address → 24bit Dummy → Data out
Fast Read Dual Output (3Bh): **3Bh** → 16bit Column Address → 8bit Dummy → Data out by 2
Fast Read Dual Output (3Ch): **3Ch** → 16bit Column Address → 24bit Dummy → Data out by 2
Fast Read Quad Output (6Bh): **6Bh** → 16bit Column Address → 8bit Dummy → Data out by 4
Fast Read Quad Output (6Ch): **6Ch** → 16bit Column Address → 24bit Dummy → Data out by 4
Fast Read Dual I/O (BBh): **BBh** → 16bit Column Address by 2 → 8bit Dummy by 2(4clocks) → Data out by 2
Fast Read Dual I/O (BCh): **BCh** → 16bit Column Address by 2 → 24bit Dummy by 2(12clocks) → Data out by 2
Fast Read Quad I/O (EBh): **EBh** → 16bit Column Address by 4 → 16bit Dummy by 4(4clocks) → Data out by 4
Fast Read Quad I/O (ECh): **EBh** → 16bit Column Address by 4 → 40bit Dummy by 4(10clocks) → Data out by 4

2.4 Page Program Sequence

2.4.1 SPI NOR(W25Q256JW):

Page Program(02h): **02h** → 24bit Address → Data In(Byte0 ~ up to Byte255)
Page Program (12h): **12h** → 32bit Address → Data In(Byte0 ~ up to Byte255)

2.4.2 SPI NAND(W25N01GW):

*. Program Execute Command(10h) has to be inserted for programming flash cells.
Page Program(02h): **02h** → 16bit Column Address → Data In(Byte0 ~ up to Byte2048) → **10h** → 8bit Dummy → 16bit Page Address

2.5 Sector/Block Erase

2.5.1 SPI NOR(W25Q256JW):

Sector Erase 4KB(20h): **20h** → 32/24bit Address
Block Erase 32KB(52h): **52h** → 32/24bit Address
Block Erase 64KB(D8h): **D8h** → 32/24bit Address

2.5.2 SPI NAND(W25N01GW):

Block Erase 128KB(D8h): **D8h** → 8bit Dummy → 16bit Page Address

2.6 Chip Erase

2.6.1 SPI NOR(W25Q256JW):

Chip Erase(C7/60h): **C7h or 60h**

2.6.2 SPI NAND(W25N01GW):

Block Erase 128KB(D8h): **D8h** → 8bit Dummy → 16bit Block Address (Block0) → **D8h** → 8bit Dummy → 16bit Block Address (repeat until Block1023)

3. Features Comparison

Summary of Features	SPI NOR(W25Q256JW)	SPI NAND(W25N01GW)
Features	BP protection	BP protection
	Individual Block protection	NA
	Hardware Reset	NA
	Software Reset	Software Reset
	Program/Erase Suspend/Resume	NA
	QPI available	NA
	Command Enter/Exit4-Byte Address	NA
	EAR(Extended Address Register)	NA
	Dedicated 4-Byte Address Commands	Dedicated 4-Byte Address Commands
	SFDP	Parameter Page
	DDR (DTR)	NA
	Uniform 4/32/64KB	Uniform 128KB
	Deep Power Down	NA
	Unique ID (64-Bit)	Unique ID (2,048 Byte)
	3x256-Byte OTP	10x2,048-Byte OTP
	Burst Read with Wrap	NA
	NA	Bad Block Management
	NA	ECC

Revision History

Version	Date	Page	Description
1.0	05/19/2017	NA	Original

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