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1. GENERAL DESCRIPTION

LPDDR2 is a high-speed SDRAM device using a double data rate architecture on the command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

For LPDDR2 devices, accesses begin with the registration of an activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

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2. LPDDR2 device power-up and initialization

The LPDDR2 Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

2.1 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory.

1. Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (=<0.2xVDDCA), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

On or before the completion of the power ramp (Tb) CKE must be held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up.CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up.

The following conditions apply:
Ta is the point where any power supply first reaches 300mV.
After Ta is reached, VDD1 must be greater than VDD2 - 200mV.
After Ta is reached, VDD1 and VDD2 must be greater than VDDCA - 200mV.
After Ta is reached, VDD1 and VDD2 must be greater than VDDQ - 200mV.

After Ta is reached, VREF must always be less than all other supply voltages.
The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100mV.
The above conditions apply between Ta and power-off (controlled or uncontrolled).

Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

Power ramp duration tINIT0 (Tb - Ta) must be no greater than 20 ms.

2. CKE and clock

Beginning at Tb, CKE must remain low for at least tINIT1 = 100 ns, after which it may be asserted high. Clock must be stable at least tINIT2 = 5 x tCK prior to the first low to high transition of CKE (Tc). CKE, CS_n and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for tCKb (18 ns to 100 ns), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings aremet. Furthermore, some AC parameters (e.g. tDQSCK) may have relaxed timings (e.g. tDQSCKb) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least tINIT3 = 200 us. (Td).

3. Reset command

After tINIT3 is satisfied, a MRW (Reset) command shall be issued (Td). **The memory controller need to issue a Pre-Charge All command prior to the MRW Reset command to make sure the LPDDR2 device is staying at IDLE state prior to the MRW Reset command being received for preventing MRW Reset command fail due to some memory bank being active caused by not well controlled input signals during power ramp up period.** Wait for at least tINIT4 = 1 μs while keeping CKE asserted and issuing NOP commands.

4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After tINIT4 is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed. Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification.

The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of tINIT5 before proceeding.

As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.

After the DAI-bit (MR0, "DAI") is set to zero "DAI complete" by the memory device, the device is in idle state(Tf). The state of the DAI status bit can be determined by an MRR command to MR0.

The LPDDR2 SDRAM device will set the DAI-bit no later than tINIT5 (10 us) after the Reset command. The memory controller shall wait a minimum of tINIT5 or until the DAI-bit is set before proceeding.

After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 "Device Information" etc.).

5. ZQ Calibration:

After tINIT5 (Tf), an MRW ZQ Initialization Calibration command may be issued to the memory. This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature variations. The MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after tZQINIT.

6. Normal Operation:

After tZQINIT (Tg), MRW commands may be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.

The LPDDR2 device will now be in IDLE state and ready for any valid command.

After Tg, the clock frequency may be changed according to the clock frequency change procedure.

2.2 Timing Parameters for initialization

Symbol	Value		Unit	Comment
	min	max		
tINIT0		20	ms	Maximum Power Ramp Time
tINIT1	100		ns	Minimum CKE low time after completion of power ramp
tINIT2	5		tCK	Minimum stable clock before first CKE high
tINIT3	200		µs	Minimum Idle time after first CKE assertion
tINIT4	1		µs	Minimum Idle time after Reset command,
tINIT5		10	µs	Maximum duration of Device Auto-Initialization
tCKb	18	100	ns	Clock cycle time during boot

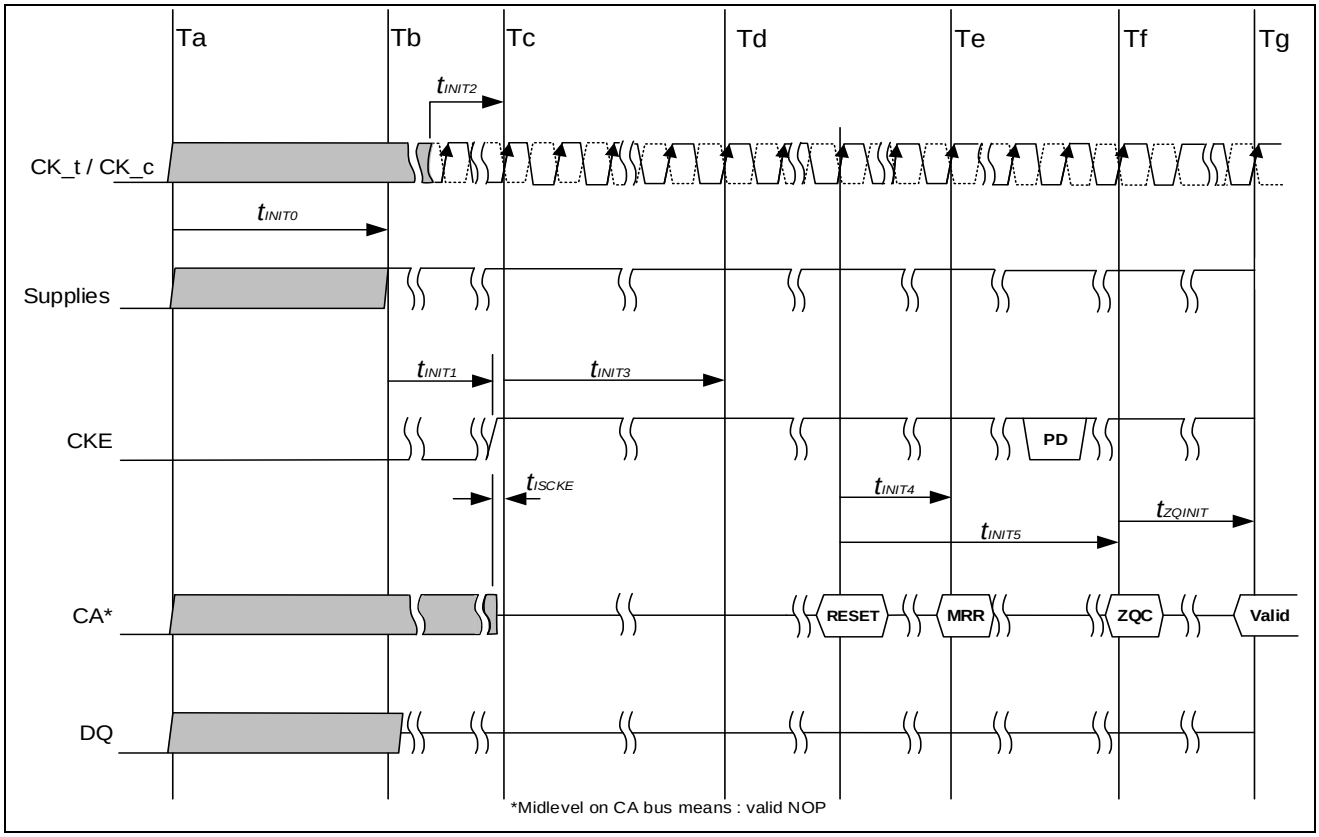

Figure of Power Ramp and Initialization Sequence

2.3 Initialization after Reset (without Power ramp)

If the RESET command is issued outside the power up initialization sequence, the re-initialization procedure shall begin with step 3 (Td).

3. Pre-Charge All Command for Power up initialization

After power supplies (VDD1, VDD2, VDDCA and VDDQ) are well power up and CKE and clock input are well set up, **the memory controller need to issue a Pre-Charge All command prior to the MRW Reset command to make sure the LPDDR2 device is staying at IDLE state prior to the MRW Reset command being received for preventing some internal circuitries being active and not effected by the MRW reset command.**

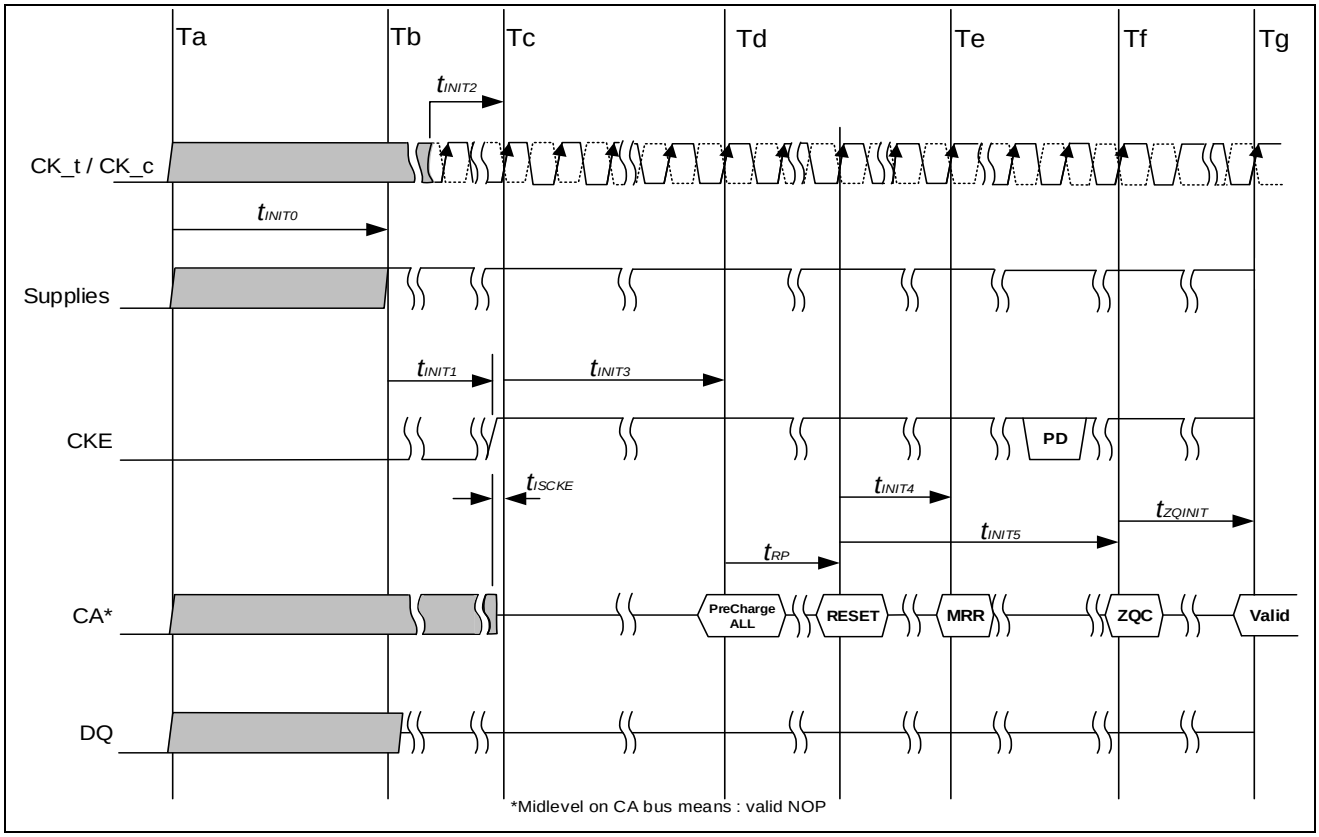

Figure of power Ramp and initialization sequence with Pre-Charge all command prior to RESET command.

4. Revision History

Version	date	Content
P01-001	2014.6.30	Initial document
P01-002	2014.7.31	Refine the timing diagram with Pre-Charge All command
P01-003	2018.10.12	Modify waveform in section 2.3
		Adding description for explaining “Pre-Charge all command power initialization in section 3.