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1. GENERAL DESCRIPTION

W9816G6JH is a high-speed synchronous dynamic random access memory (SDRAM), organized as 512K words × 2 banks × 16 bits. W9816G6JH delivers a data bandwidth of up to 200M words per second. To fully comply with the personal computer industrial standard, W9816G6JH is sorted into the following speed grades: -5, -6, -6I, -7 and -7I.

The -5 grade parts can run up to 200MHz/CL3.

The -6 and -6I grade parts can run up to 166MHz/CL3 (the -6I industrial grade parts which is guaranteed to support -40°C ≤ TA ≤ 85°C).

The -7 and -7I grade parts can run up to 143MHz/CL3 (the -7I industrial grade parts which is guaranteed to support -40°C ≤ TA ≤ 85°C).

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time.

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. W9816G6JH is ideal for main memory in high performance applications.

2. FEATURES

- 2.7V~3.6V power supply
- Up to 200 MHz Clock Frequency
- 524,288 words x 2 banks x 16 bits organization
- Self Refresh current: standard and low power
- CAS Latency: 2 and 3
- Burst Length: 1, 2, 4, 8 and Full Page
- Burst Read, Single Writes Mode
- Byte Data Controlled by LDQM, UDQM
- Auto-precharge and Controlled Precharge
- 2K Refresh Cycles/32 mS
- Interface: LVTTL
- Packaged in 50-pin, 400 mil TSOP II, using Lead free materials with RoHS compliant
3. ORDER INFORMATION

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>SPEED GRADE</th>
<th>SELF REFRESH CURRENT (MAX)</th>
<th>OPERATING TEMPERATURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>W9816G6JH-5</td>
<td>200MHz/CL3</td>
<td>2mA</td>
<td>0°C ~ 70°C</td>
</tr>
<tr>
<td>W9816G6JH-6</td>
<td>166MHz/CL3</td>
<td>2mA</td>
<td>0°C ~ 70°C</td>
</tr>
<tr>
<td>W9816G6JH-6I</td>
<td>166MHz/CL3</td>
<td>2mA</td>
<td>-40°C ~ 85°C</td>
</tr>
<tr>
<td>W9816G6JH-7</td>
<td>143MHz/CL3</td>
<td>2mA</td>
<td>0°C ~ 70°C</td>
</tr>
<tr>
<td>W9816G6JH-7I</td>
<td>143MHz/CL3</td>
<td>2mA</td>
<td>-40°C ~ 85°C</td>
</tr>
</tbody>
</table>

4. PIN CONFIGURATION

```
VDD  1
DQ0  2
DQ1  3
VSSQ 4
DQ2  5
DQ3  6
VDDQ 7
DQ4  8
DQ5  9
VSSQ 10
DQ6 11
DQ7 12
VDDQ 13
LDQM 14
WE 15
CAS 16
RAS 17
CS 18
BA 19
A10 20
A9 21
A10 22
A8 23
A9 24
A7 25
VDD 26
DQ15 49
DQ14 48
VSSQ 47
DQ13 46
DQ12 45
VDDQ 44
DQ11 43
DQ10 42
VSSQ 41
DQ9 40
DQ8 39
VDDQ 38
NC 37
UDQM 36
CLK 35
CE 34
NC 33
A9 32
A8 31
A7 30
A6 29
A5 28
A4 27
VSS 26
```
## 5. PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN NUMBER</th>
<th>PIN NAME</th>
<th>FUNCTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>21, 22, 23, 24, 27, 28, 29, 30, 31, 32, 20</td>
<td>A0–A10</td>
<td>Address</td>
<td>Multiplexed pins for row and column address. Row address: A0–A10. Column address: A0–A7.</td>
</tr>
<tr>
<td>19</td>
<td>BA</td>
<td>Bank Select</td>
<td>Select bank to activate during row address latch time, or bank to read/write during column address latch time.</td>
</tr>
<tr>
<td>2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 44, 46, 48, 49</td>
<td>DQ0–DQ15</td>
<td>Data Input/Output</td>
<td>Multiplexed pins for data input and output.</td>
</tr>
<tr>
<td>18</td>
<td>ĖCS</td>
<td>Chip Select</td>
<td>Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.</td>
</tr>
<tr>
<td>17</td>
<td>ĖRAS</td>
<td>Row Address Strobe</td>
<td>Command input. When sampled at the rising edge of the clock, ĖRAS, ĖCAS and ĖWE define the operation to be executed.</td>
</tr>
<tr>
<td>16</td>
<td>ĖCAS</td>
<td>Column Address Strobe</td>
<td>Referred to ĖRAS</td>
</tr>
<tr>
<td>15</td>
<td>ĖWE</td>
<td>Write Enable</td>
<td>Referred to ĖRAS</td>
</tr>
<tr>
<td>36, 14</td>
<td>UDQM/ LDQM</td>
<td>Input/Output Mask</td>
<td>The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.</td>
</tr>
<tr>
<td>35</td>
<td>CLK</td>
<td>Clock Inputs</td>
<td>System clock used to sample inputs on the rising edge of clock.</td>
</tr>
<tr>
<td>34</td>
<td>CKE</td>
<td>Clock Enable</td>
<td>CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.</td>
</tr>
<tr>
<td>1, 25</td>
<td>ĖVDD</td>
<td>Power</td>
<td>Power for input buffers and logic circuit inside DRAM.</td>
</tr>
<tr>
<td>26, 50</td>
<td>ĖVSS</td>
<td>Ground</td>
<td>Ground for input buffers and logic circuit inside DRAM.</td>
</tr>
<tr>
<td>7, 13, 38, 44,</td>
<td>ĖVDDQ</td>
<td>Power for I/O buffer</td>
<td>Separated power from ĖVDD, used for output buffers to improve noise immunity.</td>
</tr>
<tr>
<td>4, 10, 41, 47</td>
<td>ĖVSSQ</td>
<td>Ground for I/O buffer</td>
<td>Separated ground from ĖVSS, used for output buffers to improve noise immunity.</td>
</tr>
<tr>
<td>33, 37</td>
<td>NC</td>
<td>No Connection</td>
<td>No connection.</td>
</tr>
</tbody>
</table>
6. BLOCK DIAGRAM

Note: The cell array configuration is 2048 * 256 * 16
7. FUNCTIONAL DESCRIPTION

7.1 Power Up and Initialization

The default power up state of the mode register is unspecified. The following power up and initialization sequence need to be followed to guarantee the device being preconditioned to each user specific needs during power up, all VDD and VDDQ pins must be ramp up simultaneously to the specified voltage when the input signals are held in the “NOP" state. The power up voltage must not exceed VDD + 0.3V on any of the input pins or VDD supplies. After power up, an initial pause of 200 µS is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power up, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. An additional eight Auto Refresh cycles (CBR) are also required before or after programming the Mode Register to ensure proper subsequent operation.

7.2 Programming Mode Register

After initial power up, the Mode Register Set Command must be issued for proper device operation. All banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The Mode Register Set Command is activated by the low signals of RAS, CAS, CS and WE at the positive edge of the clock. The address input data during this cycle defines the parameters to be set as shown in the Mode Register Operation table. A new command may be issued following the mode register set command once a delay equal to tRSC has elapsed. Please refer to the next page for Mode Register Set Cycle and Operation Table.

7.3 Bank Activate Command

The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from when the Bank Activate command is applied to when the first read or write operation can begin must not be less than the RAS to CAS delay time (tRCD). Once a bank has been activated it must be precharged before another Bank Activate command can be issued to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank-to-Bank delay time (tRRD). The maximum time that each bank can be held active is specified as tRAS(max.).

7.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be followed. This is accomplished by setting RAS high and CAS low at the clock rising edge after minimum of tRCD delay. WE pin voltage level defines whether the access cycle is a read operation (WE high), or a write operation (WE low). The address inputs determine the starting column address. Reading or writing to a different row within an activated bank requires the bank be precharged and a new Bank Activate command be issued. When more than one bank is activated, interleaved bank Read or Write operations are possible. By using the programmed burst length and alternating the access and precharge operations between multiple banks, seamless data access operation among many different pages can be realized. Read or Write Commands can also be issued to the same bank or between active banks on every clock cycle.
7.5 Burst Read Command

The Burst Read command is initiated by applying logic low level to CS and CAS while holding RAS and WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The Mode Register sets type of burst (sequential or interleave) and the burst length (1, 2, 4, 8 and full page) during the Mode Register Set Up cycle.

7.6 Burst Write Command

The Burst Write command is initiated by applying logic low level to CS, CAS and WE while holding RAS high at the rising edge of the clock. The address inputs determine the starting column address. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. Data supplied to the DQ pins after burst finishes will be ignored.

7.7 Read Interrupted by a Read

A Burst Read may be interrupted by another Read Command. When the previous burst is interrupted, the remaining addresses are overridden by the new read address with the full burst length. The data from the first Read Command continues to appear on the outputs until the CAS Latency from the interrupting Read Command is satisfied.

7.8 Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM may be needed to place the DQs (output drivers) in a high impedance state to avoid data contention on the DQ bus. If a Read Command will issue data on the first and second clock cycles of the write operation, DQM is needed to insure the DQs are tri-stated. After that point the Write Command will have control of the DQ bus and DQM masking is no longer needed.

7.9 Write Interrupted by a Write

A burst write may be interrupted before completion of the burst by another Write Command. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

7.10 Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is activated. The DQs must be in the high impedance state at least one cycle before the new read data appears on the outputs to avoid data contention. When the Read Command is activated, any residual data from the burst write cycle will be ignored.
7.11 Burst Stop Command

A Burst Stop Command may be used to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank, if the burst length is full page. Use of the Burst Stop Command during other burst length operations is illegal. The Burst Stop Command is defined by having RAS and CAS high with CS and WE low at the rising edge of the clock. The data DQs go to a high impedance state after a delay, which is equal to the CAS Latency in a burst read cycle, interrupted by Burst Stop. If a Burst Stop Command is issued during a full page burst write operation, then any residual data from the burst write cycle will be ignored.

7.12 Addressing Sequence of Sequential Mode

A column access is performed by increasing the address from the column address, which is input to the device. The disturb address is varied by the Burst Length as shown in Table 2.

<table>
<thead>
<tr>
<th>DATA</th>
<th>ACCESS ADDRESS</th>
<th>BURST LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data 0</td>
<td>n</td>
<td>BL = 2 (disturb address is A0)</td>
</tr>
<tr>
<td>Data 1</td>
<td>n + 1</td>
<td>No address carry from A0 to A1</td>
</tr>
<tr>
<td>Data 2</td>
<td>n + 2</td>
<td>BL = 4 (disturb addresses are A0 and A1)</td>
</tr>
<tr>
<td>Data 3</td>
<td>n + 3</td>
<td>No address carry from A1 to A2</td>
</tr>
<tr>
<td>Data 4</td>
<td>n + 4</td>
<td></td>
</tr>
<tr>
<td>Data 5</td>
<td>n + 5</td>
<td>BL = 8 (disturb addresses are A0, A1 and A2)</td>
</tr>
<tr>
<td>Data 6</td>
<td>n + 6</td>
<td>No address carry from A2 to A3</td>
</tr>
<tr>
<td>Data 7</td>
<td>n + 7</td>
<td></td>
</tr>
</tbody>
</table>

7.13 Addressing Sequence of Interleave Mode

A column access is started in the input column address and is performed by inverting the address bit in the sequence shown in Table 3.

<table>
<thead>
<tr>
<th>DATA</th>
<th>ACCESS ADDRESS</th>
<th>BURST LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data 0</td>
<td>A8 A7 A6 A5 A4 A3 A2 A1 A0</td>
<td>BL = 2</td>
</tr>
<tr>
<td>Data 1</td>
<td>A8 A7 A6 A5 A4 A3 A2 A1 A0</td>
<td></td>
</tr>
<tr>
<td>Data 2</td>
<td>A8 A7 A6 A5 A4 A3 A2 A1 A0</td>
<td>BL = 4</td>
</tr>
<tr>
<td>Data 3</td>
<td>A8 A7 A6 A5 A4 A3 A2 A1 A0</td>
<td></td>
</tr>
<tr>
<td>Data 4</td>
<td>A8 A7 A6 A5 A4 A3 A2 A1 A0</td>
<td>BL = 8</td>
</tr>
<tr>
<td>Data 5</td>
<td>A8 A7 A6 A5 A4 A3 A2 A1 A0</td>
<td></td>
</tr>
<tr>
<td>Data 6</td>
<td>A8 A7 A6 A5 A4 A3 A2 A1 A0</td>
<td></td>
</tr>
<tr>
<td>Data 7</td>
<td>A8 A7 A6 A5 A4 A3 A2 A1 A0</td>
<td></td>
</tr>
</tbody>
</table>
7.14 Auto-precharge Command

If A10 is set to high when the Read or Write Command is issued, then the Auto-precharge function is entered. During Auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge automatically before all burst read cycles have been completed. Regardless of burst length, it will begin a certain number of clocks prior to the end of the scheduled burst cycle. The number of clocks is determined by CAS Latency.

A Read or Write Command with Auto-precharge can not be interrupted before the entire burst operation is completed. Therefore, use of a Read, Write, or Precharge Command is prohibited during a read or write cycle with Auto-precharge. Once the precharge operation has started, the bank cannot be reactivated until the Precharge time ($t_{RP}$) has been satisfied. Issue of Auto-precharge command is illegal if the burst is set to full page length. If A10 is high when a Write Command is issued, the Write with Auto-precharge function is initiated. The SDRAM automatically enters the precharge operation two clock delay from the last burst write cycle. This delay is referred to as Write $t_{WR}$. The bank undergoing Auto-precharge can not be reactivated until $t_{WR}$ and $t_{RP}$ are satisfied. This is referred to as $t_{DAL}$, Data-in to Active delay ($t_{DAL} = t_{WR} + t_{RP}$). When using the Auto-precharge Command, the interval between the Bank Activate Command and the beginning of the internal precharge operation must satisfy $t_{RAS}(\text{min})$.

7.15 Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is entered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or all banks simultaneously. The address bits, A10, and BA, are used to define which bank(s) is to be precharged when the command is issued. After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time ($t_{RP}$).

7.16 Self Refresh Command

The Self-Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. All banks must be idle prior to issuing the Self-Refresh Command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self-Refresh Operation to save power. The device will exit Self-Refresh operation after CKE is returned high. Any subsequent commands can be issued after $t_{XSR}$ from the end of Self Refresh command.
7.17 Power Down Mode
The Power Down mode is initiated by holding CKE low. All of the receiver circuits except CKE are gated off to reduce the power. The Power Down mode does not perform any refresh operations; therefore the device can not remain in Power Down mode longer than the Refresh period (tREF) of the device.

The Power Down mode is exited by bringing CKE high. When CKE goes high, a No Operation Command is required on the next rising clock edge, depending on tCK. The input buffers need to be enabled with CKE held high for a period equal to tCKS(min) + tCK(min).

7.18 No Operation Command
The No Operation Command should be used in cases when the SDRAM is in an idle or a wait state to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when CS is low with RAS, CAS and WE held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

7.19 Deselect Command
The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when CS is brought high, the RAS, CAS and WE signals become don't cares.

7.20 Clock Suspend Mode
During normal access mode, CKE must be held high enabling the clock. When CKE is registered low while at least one of the banks is active and a column access/burst is in progress, Clock Suspend mode is entered. The Clock Suspend mode deactivates the internal clock and suspends any clocked operation that was currently being executed. There is a one-clock delay between the registration of CKE low and the time at which the SDRAM operation suspends. While in Clock Suspend mode, the SDRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one-clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.
8. OPERATION MODE

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 1 shows the truth table for the operation commands.

Table 1 Truth Table (Note 1, 2)

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>DEVICE STATE</th>
<th>CKEn-1</th>
<th>CKEn</th>
<th>DQM</th>
<th>BA</th>
<th>A10</th>
<th>A9-A0</th>
<th>CS</th>
<th>RAS</th>
<th>CAS</th>
<th>WE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank Active</td>
<td>Idle</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Bank Precharge</td>
<td>Any</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>V</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>Precharge All</td>
<td>Any</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Write</td>
<td>Active (3)</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>V</td>
<td>L</td>
<td>V</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Write with Auto-precharge</td>
<td>Active (3)</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>V</td>
<td>H</td>
<td>V</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Read</td>
<td>Active (3)</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>V</td>
<td>L</td>
<td>V</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>Read with Auto-precharge</td>
<td>Active (3)</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>V</td>
<td>H</td>
<td>V</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>Mode Register Set</td>
<td>Idle</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>No-Operation</td>
<td>Any</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Burst Stop</td>
<td>Active (4)</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>Device Deselect</td>
<td>Any</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Auto-Refresh</td>
<td>Idle</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>Self-Refresh Entry</td>
<td>Idle</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>Self-Refresh Exit</td>
<td>Idle (S.R)</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Clock Suspend Mode</td>
<td>Active</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Entry</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Down Mode Entry</td>
<td>Idle (Active (5))</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Clock Suspend Mode</td>
<td>Active</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Exit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Down Mode Exit</td>
<td>Any (power down)</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Data Write/Output Enable</td>
<td>Active</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Data Write/Output Disable</td>
<td>Active</td>
<td>H</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Notes:

1. V = valid, X = Don't care, L = Low Level, H = High Level
2. CKEn signal is input level when commands are provided.
   CKEn-1 signal is the input level one clock cycle before the command is issued.
3. These are state of bank designated by BA signals.
4. Device state is full page burst operation.
5. Power Down Mode can not be entered in the burst cycle.
   When this command asserts in the burst cycle, device state is clock suspend mode.
9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>RATING</th>
<th>UNIT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage on any pin relative to VSS</td>
<td>VIN, VOUT</td>
<td>-0.5 ~ VDD + 0.5 (≤ 4.6V max.)</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Voltage on VDD/VDDQ supply relative to VSS</td>
<td>VDD, VDDQ</td>
<td>-0.5 ~ 4.6</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Operating Temperature for -5/-6/-7</td>
<td>TA</td>
<td>0 ~ 70</td>
<td>°C</td>
<td>1</td>
</tr>
<tr>
<td>Operating Temperature for -6/-7</td>
<td>TA</td>
<td>-40 ~ 85</td>
<td>°C</td>
<td>1</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>TSTG</td>
<td>-55 ~ 150</td>
<td>°C</td>
<td>1</td>
</tr>
<tr>
<td>Soldering Temperature (10s)</td>
<td>TSOLDER</td>
<td>260</td>
<td>°C</td>
<td>1</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>PD</td>
<td>1</td>
<td>W</td>
<td>1</td>
</tr>
<tr>
<td>Short Circuit Output Current</td>
<td>IOUT</td>
<td>50</td>
<td>mA</td>
<td>1</td>
</tr>
</tbody>
</table>

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9.2 Recommended DC Operating Conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYM.</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>VDD</td>
<td>2.7</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Power Supply Voltage (for I/O Buffer)</td>
<td>VDDQ</td>
<td>2.7</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>VIH</td>
<td>2.0</td>
<td>-</td>
<td>VDD + 0.3</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>VIL</td>
<td>-0.3</td>
<td>-</td>
<td>0.8</td>
<td>V</td>
<td>2</td>
</tr>
</tbody>
</table>

Note: \( V_{IH}(\text{max.}) = V_{DD}/V_{DDQ} + 1.5V \) for pulse width \( \leq 5 \) nS
\( V_{IL}(\text{min.}) = V_{SS}/V_{SSQ} - 1.5V \) for pulse width \( \leq 5 \) nS

9.3 Capacitance

\( V_{DD} = 2.7V~3.6V \), \( T_A = 25^\circ C \), \( f = 1MHz \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYM.</th>
<th>MIN.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance (A0 to A10, BA, CS, RAS, CAS, WE, UDQM, LDQM, CKE)</td>
<td>CI</td>
<td>-</td>
<td>4</td>
<td>pf</td>
</tr>
<tr>
<td>Input Capacitance (CLK)</td>
<td>CCLK</td>
<td>-</td>
<td>4</td>
<td>pf</td>
</tr>
<tr>
<td>Input/Output capacitance (DQ0 to DQ15)</td>
<td>CIO</td>
<td>-</td>
<td>5.5</td>
<td>pf</td>
</tr>
</tbody>
</table>

Note: These parameters are periodically sampled and not 100% tested.
## 9.4 DC Characteristics

\( \text{VDD} = 2.7 \text{V to 3.8V}, \ T_A = 0 \text{ to 70°C for } -5/-6/-7, \ T_A = -40 \text{ to 85°C for } -6/-7I \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYM.</th>
<th>-5</th>
<th>-6/-6I</th>
<th>-7/-7I</th>
<th>UNIT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Current</td>
<td>( t_{\text{CK}} = \text{min.}, \ t_{\text{RC}} = \text{min.} ) Active precharge command cycling without burst operation</td>
<td>1 Bank operation</td>
<td>( I_{\text{DD1}} )</td>
<td>40</td>
<td>35</td>
<td>30</td>
</tr>
<tr>
<td>Standby Current</td>
<td>( t_{\text{CK}} = \text{min.}, \ \overline{\text{CS}} = \text{VIH} ) ( \text{VIH/L} = \text{VIH} ) (min.)/VIL (max.)</td>
<td>( CKE = \text{VIH} )</td>
<td>( I_{\text{DD2}} )</td>
<td>15</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>Bank: Inactive state</td>
<td>( CKE = \text{VIL} ) (Power Down Mode)</td>
<td>( I_{\text{DD2P}} )</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>mA</td>
</tr>
<tr>
<td>Standby Current</td>
<td>( \text{CLK} = \text{VIH}, \ \overline{\text{CS}} = \text{VIH} ) ( \text{VIH/L} = \text{VIH} ) (min.)/VIL (max.)</td>
<td>( CKE = \text{VIH} )</td>
<td>( I_{\text{DD2S}} )</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Bank: Inactive state</td>
<td>( CKE = \text{VIL} ) (Power Down Mode)</td>
<td>( I_{\text{DD2PS}} )</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>mA</td>
</tr>
<tr>
<td>No Operating Current</td>
<td>( t_{\text{CK}} = \text{min.}, \ \overline{\text{CS}} = \text{VIH} ) (min)</td>
<td>( CKE = \text{VIH} )</td>
<td>( I_{\text{DD3}} )</td>
<td>25</td>
<td>23</td>
<td>20</td>
</tr>
<tr>
<td>Bank: Active state (2 Banks)</td>
<td>( CKE = \text{VIL} ) (Power Down Mode)</td>
<td>( I_{\text{DD3P}} )</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>mA</td>
</tr>
<tr>
<td>Burst Operating Current</td>
<td>( t_{\text{CK}} = \text{min.} ) Read/Write command cycling</td>
<td>( I_{\text{DD4}} )</td>
<td>60</td>
<td>55</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>Auto Refresh Current</td>
<td>( t_{\text{CK}} = \text{min.} ) Auto refresh command cycling</td>
<td>( I_{\text{DD5}} )</td>
<td>45</td>
<td>40</td>
<td>35</td>
<td>mA</td>
</tr>
<tr>
<td>Self Refresh Current</td>
<td>Self Refresh Mode</td>
<td>( CKE = 0.2V )</td>
<td>( I_{\text{DD6}} )</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYM.</th>
<th>MIN.</th>
<th>MAX.</th>
<th>UNIT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Leakage Current</td>
<td>( \text{0V} \leq \text{VIN} \leq \text{VDD}, \text{ all other pins not under test} = 0V )</td>
<td>( I_{\text{IL}} )</td>
<td>-5</td>
<td>5</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>( \text{Output disable, } 0V \leq \text{VOUT} \leq \text{VDDQ} )</td>
<td>( I_{\text{OL}} )</td>
<td>-5</td>
<td>5</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>LVTTL Output “H” Level Voltage</td>
<td>( I_{\text{OUT}} = -2 \text{mA} )</td>
<td>( V_{\text{OH}} )</td>
<td>2.4</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>LVTTL Output “L” Level Voltage</td>
<td>( I_{\text{OUT}} = 2 \text{mA} )</td>
<td>( V_{\text{OL}} )</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
</tr>
</tbody>
</table>
### 9.5 AC Characteristics

\[(V_{DD} = 2.7V \text{ to } 3.6V, T_A = 0 \text{ to } 70°C \text{ for } -5/-6/-7, T_A = -40 \text{ to } 85°C \text{ for } -6/-7/-7)\]

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYM.</th>
<th>-5</th>
<th>-6/-6I</th>
<th>-7/-7I</th>
<th>UNIT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ref/Active to Ref/Active Command Period</td>
<td>tRC</td>
<td>55</td>
<td>60</td>
<td>65</td>
<td>nS</td>
<td></td>
</tr>
<tr>
<td>Active to Precharge Command Period</td>
<td>tRAS</td>
<td>40</td>
<td>100000</td>
<td>42</td>
<td>100000</td>
<td></td>
</tr>
<tr>
<td>Active to Read/Write Command Delay Time</td>
<td>tRCD</td>
<td>15</td>
<td>18</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read/Write(a) to Read/Write(b) Command Period</td>
<td>tCD</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>tCK</td>
<td></td>
</tr>
<tr>
<td>Precharge to Active(b) Command Period</td>
<td>tAP</td>
<td>15</td>
<td>18</td>
<td>18</td>
<td>nS</td>
<td></td>
</tr>
<tr>
<td>Active(a) to Active(b) Command Period</td>
<td>tRD</td>
<td>10</td>
<td>12</td>
<td>14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Write Recovery Time</td>
<td>CL* = 2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>tCK</td>
<td></td>
</tr>
<tr>
<td>CLK Cycle Time</td>
<td>CL* = 2</td>
<td>71000</td>
<td>81000</td>
<td>101000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK High Level Width</td>
<td>CL* = 2</td>
<td>51000</td>
<td>61000</td>
<td>71000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK Low Level Width</td>
<td>CL* = 2</td>
<td>2222</td>
<td>2222</td>
<td>2222</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Access Time from CLK</td>
<td>CL* = 2</td>
<td>65.5</td>
<td>5.5</td>
<td>5.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Data Hold Time</td>
<td>CL* = 3</td>
<td>4.55</td>
<td>55</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Data High Impedance Time</td>
<td>CL* = 2</td>
<td>65.5</td>
<td>5.5</td>
<td>5.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Data Low Impedance Time</td>
<td>CL* = 3</td>
<td>4.55</td>
<td>55</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Down Mode Entry Time</td>
<td>tSB</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>Data-in-Set-up Time</td>
<td>tDQS</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data-in Hold Time</td>
<td>tDH</td>
<td>0.7</td>
<td>0.7</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address Set-up Time</td>
<td>tAS</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>tAH</td>
<td>0.7</td>
<td>0.7</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CKE Set-up Time</td>
<td>tCKS</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CKE Hold Time</td>
<td>tCKH</td>
<td>0.7</td>
<td>0.7</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Command Set-up Time</td>
<td>tCMS</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Command Hold Time</td>
<td>tCMH</td>
<td>0.7</td>
<td>0.7</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Refresh Time (2K Refresh Cycles)</td>
<td>tREF</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>mS</td>
<td></td>
</tr>
<tr>
<td>Mode Register Set Cycle Time</td>
<td>tRSC</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>tCK</td>
<td></td>
</tr>
<tr>
<td>Exit self refresh to ACTIVE command</td>
<td>tMSR</td>
<td>70</td>
<td>72</td>
<td>75</td>
<td>nS</td>
<td></td>
</tr>
</tbody>
</table>

* CL = CAS Latency
Notes:
1. Operation exceeds "Absolute Maximum Ratings" may cause permanent damage to the devices.
2. All voltages are referenced to Vss.
3. These parameters depend on the cycle rate and listed values are measured at a cycle rate with the minimum values of tCK and tRC.
4. These parameters depend on the output loading conditions. Specified values are obtained with output open.
5. Power up sequence please refer to "Functional Description" section described before.
6. AC test load diagram.

```
AC TEST LOAD

1.4 V
50 ohms

output
Z = 50 ohms
30pF
```

7. \( t_{HZ} \) defines the time at which the outputs achieve the open circuit condition and is not referenced to output level.
8. Assumed input rise and fall time \( (t_{r}) = 1\, \text{nS} \).
   If \( t_r \& t_f \) is longer than 1nS, transient time compensation should be considered, i.e., \([(t_r + t_f)/2 - 1]\)nS should be added to the parameter.
9. If clock rising time \( (t_C) \) is longer than 1nS, \((t_C/2-0.5)\)nS should be added to the parameter.
10. TIMING WAVEFORMS

10.1 Command Input Timing
10.2 Read Timing

- Read CAS Latency
- Burst Length
- Read Command
- Valid Data-Out
- IAC
- IHZ
- IL2
- ICH
- TOH
- TOH
- Valid Data-Out
- Burst Length

Timing parameters:
- tAC
- tLZ
- tAC
- tOH
- tHZ
- tOH

Signal lines:
- CLK
- CS
- RAS
- CAS
- WE
- A0-A10
- BA
- DQ

Data Valid
Data-Out

---

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10.3 Control Timing of Input/Output Data

**Control Timing of Input Data**
*(Word Mask)*

- **CLK**
- **DQM**
- **DQ0-15**

**Control Timing of Output Data**
*(Output Enable)*

- **CLK**
- **DQM**
- **DQ0-15**

**(Clock Mask)**

- **CLK**
- **CKE**
- **DQ0-15**
10.4 Mode Register Set Cycle

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Value</th>
<th>Burst Length</th>
<th>CAS Latency</th>
<th>Addressing Mode</th>
<th>Write Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Burst Length</td>
<td>A2 A1 A0</td>
<td>Sequential</td>
<td>Interleave</td>
<td>A2 A1 A0</td>
<td>A2 A1 A0</td>
</tr>
<tr>
<td>A1</td>
<td></td>
<td>0 0 0</td>
<td>1</td>
<td>1</td>
<td>0 0 0</td>
<td>0 0 0</td>
</tr>
<tr>
<td>A2</td>
<td></td>
<td>0 0 1</td>
<td>2</td>
<td>2</td>
<td>0 0 1</td>
<td>0 0 1</td>
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<tr>
<td>A3</td>
<td>Addressing Mode</td>
<td>0 1 0</td>
<td>4</td>
<td>4</td>
<td>0 1 0</td>
<td>0 1 0</td>
</tr>
<tr>
<td>A4</td>
<td></td>
<td>0 1 1</td>
<td>8</td>
<td>8</td>
<td>0 1 1</td>
<td>0 1 1</td>
</tr>
<tr>
<td>A5</td>
<td>CAS Latency</td>
<td>1 0 0</td>
<td>Reserved</td>
<td>Reserved</td>
<td>1 0 0</td>
<td>1 0 0</td>
</tr>
<tr>
<td>A6</td>
<td></td>
<td>1 0 1</td>
<td>Reserved</td>
<td>Reserved</td>
<td>1 0 1</td>
<td>1 0 1</td>
</tr>
<tr>
<td>A7</td>
<td>&quot;0&quot; (Test Mode)</td>
<td>1 1 0</td>
<td>Full Page</td>
<td></td>
<td>1 1 0</td>
<td>1 1 0</td>
</tr>
<tr>
<td>A8</td>
<td>&quot;0&quot; Reserved</td>
<td>1 1 1</td>
<td></td>
<td></td>
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<td>1 1 1</td>
</tr>
<tr>
<td>A9</td>
<td>Write Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A9</td>
</tr>
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<td></td>
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<tr>
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</tr>
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</table>

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11. OPERATING TIMING EXAMPLE

11.1 Interleaved Bank Read (Burst Length = 4, CAS Latency = 3)
11.2 Interleaved Bank Read (Burst Length = 4, CAS Latency = 3, Auto-precharge)

* AP is the internal precharge start timing
11.3 Interleaved Bank Read (Burst Length = 8, CAS Latency = 3)
11.4 Interleaved Bank Read (Burst Length = 8, CAS Latency = 3, Auto-precharge)

* AP is the internal precharge start timing
11.5 Interleaved Bank Write (Burst Length = 8)

* AP is the internal precharge start timing
11.6 Interleaved Bank Write (Burst Length = 8, Auto-precharge)

* AP is the internal precharge start timing
11.7 Page Mode Read (Burst Length = 4, CAS Latency = 3)

* AP is the internal precharge start timing
11.8 Page Mode Read / Write (Burst Length = 8, CAS Latency = 3)
11.9 Auto Precharge Read (Burst Length = 4, CAS Latency = 3)

* AP is the internal precharge start timing
11.10  Auto Precharge Write (Burst Length = 4)

* AP is the internal precharge start timing
11.11 Auto Refresh Cycle

All Banks Precharge
Auto Refresh

Auto Refresh (Arbitrary Cycle)
11.12 Self Refresh Cycle

CLK
CS
RAS
CAS
WE
BA
A10
A0-A9
DQM
CKE
DQ

All Banks Precharge
Self Refresh Entry
Self Refresh Exit
No Operation / Command Inhibit
Arbitrary Cycle

Self Refresh Cycle

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11.13 Burst Read and Single Write (Burst Length = 4, CAS Latency = 3)
11.14 Power Down Mode

Note: The Power Down Mode is entered by asserting CKE "low".
All input/output buffers (except CKE buffers) are turned off in the Power Down mode.
When CKE goes high, command input must be No operation at next CLK rising edge.
Violating refresh requirements during power-down may result in a loss of data.
11.15 Auto-precharge Timing (Read Cycle)

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precharging must be at least $t_{RAS}$ (min).

Note:
- $\text{Read}$ represents the Read with Auto precharge command.
- $\text{AP}$ represents the start of internal precharging.
- $\text{Act}$ represents the Bank Activate command.

(burst length = 1) Command
- (a) burst length ≤ 1
- (b) burst length ≤ 2
- (c) burst length ≤ 4
- (d) burst length ≤ 8

(burst length = 2) Command
- (a) burst length ≤ 1
- (b) burst length ≤ 2
- (c) burst length ≤ 4
- (d) burst length ≤ 8

(burst length = 4) Command
- (a) burst length ≤ 1
- (b) burst length ≤ 2
- (c) burst length ≤ 4
- (d) burst length ≤ 8

(burst length = 8) Command
- (a) burst length ≤ 1
- (b) burst length ≤ 2
- (c) burst length ≤ 4
- (d) burst length ≤ 8
11.16 Auto-precharge Timing (Write Cycle)

When the /auto precharge command is asserted, the period from Bank Activate command to the start of internal precharging must be at least tRAS (min).

Note:
- Write represents the Write with Auto precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Active command.
11.17 Timing Chart of Read to Write Cycle

In the case of Burst Length = 4

(1) CAS Latency=2
(a) Command

DQM
DQ
D0
D1
D2
D3
(Read) (Write)

(b) Command

DQM
DQ
D0
D1
D2
D3
(Read) (Write)

(2) CAS Latency=3
(a) Command

DQM
DQ
D0
D1
D2
D3
(Read) (Write)

(b) Command

DQM
DQ
D0
D1
D2
D3
(Read) (Write)

Note: The Output data must be masked by DQM to avoid I/O conflict

11.18 Timing Chart of Write to Read Cycle

In the case of Burst Length=4

(1) CAS Latency=2
(a) Command

DQM
DQ
D0
Q0
Q1
Q2
Q3
(Write) (Read)

(b) Command

DQM
DQ
D0
Q0
Q1
Q2
Q3
(Write) (Read)

(2) CAS Latency=3
(a) Command

DQM
DQ
D0
Q0
Q1
Q2
Q3
(Write) (Read)

(b) Command

DQM
DQ
D0
Q0
Q1
Q2
Q3
(Write) (Read)
11.19 Timing Chart of Burst Stop Cycle (Burst Stop Command)

![Timing Chart of Burst Stop Cycle (Burst Stop Command)]

Note: (BST) represents the Burst stop command

11.20 Timing Chart of Burst Stop Cycle (Precharge Command)

![Timing Chart of Burst Stop Cycle (Precharge Command)]
11.21 CKE/DQM Input Timing (Write Cycle)
11.22 CKE/DQM Input Timing (Read Cycle)

CLK cycle No.

External

Internal

CKE

DQM

DQ

Q1 Q2 Q3 Q4

Open

Q6

(1)

CLK cycle No.

External

Internal

CKE

DQM

DQ Q5 Q4

Q4

CLK

CLK

CLK

(2)

CLK cycle No.

External

Internal

CKE

DQM

DQ Q1 Q2 Q3 Q4 Q5 Q6

(3)
12. PACKAGE SPECIFICATION
Package Outline TSOP (TYPE II) 50L 400 mil

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DIMENSION (MM)</th>
<th>DIMENSION (INCH)</th>
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<tbody>
<tr>
<td></td>
<td>MIN.</td>
<td>NOM.</td>
</tr>
<tr>
<td>A</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>---</td>
</tr>
<tr>
<td>A2</td>
<td>0.95</td>
<td>1.00</td>
</tr>
<tr>
<td>b</td>
<td>0.30</td>
<td>---</td>
</tr>
<tr>
<td>c</td>
<td>0.12</td>
<td>---</td>
</tr>
<tr>
<td>D</td>
<td>20.82</td>
<td>20.95</td>
</tr>
<tr>
<td>HE</td>
<td>11.56</td>
<td>11.76</td>
</tr>
<tr>
<td>E</td>
<td>10.03</td>
<td>10.16</td>
</tr>
<tr>
<td>y</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>L</td>
<td>0.40</td>
<td>0.50</td>
</tr>
<tr>
<td>L1</td>
<td>---</td>
<td>0.80</td>
</tr>
<tr>
<td>θ</td>
<td>0°</td>
<td>---</td>
</tr>
<tr>
<td>ZD</td>
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SEATING PLANE

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## 13. REVISION HISTORY

<table>
<thead>
<tr>
<th>VERSION</th>
<th>DATE</th>
<th>PAGE</th>
<th>DESCRIPTION</th>
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<tr>
<td>A01</td>
<td>Jun. 24, 2014</td>
<td>All</td>
<td>Initial formally datasheet</td>
</tr>
<tr>
<td>A02</td>
<td>Dec. 27, 2016</td>
<td>41</td>
<td>Update TSOP II 50L symbol “A2” min./max. spec, symbol “θ” max. spec and symbol “c” spec</td>
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<td></td>
<td></td>
<td>42</td>
<td>Remove important notice</td>
</tr>
<tr>
<td>A03</td>
<td>Mar. 08, 2019</td>
<td>3, 13~16</td>
<td>Revise -5, -6 and -6I speed grade parts power supply voltage from 3.3V ± 0.3V to 2.7V~3.6V</td>
</tr>
</tbody>
</table>